# MILLIMETER WAVE INTEGRATED SILICON TRANSCEIVER DESIGN FOR HIGH DATA RATE COMMUNICATIONS

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# MILLIMETER WAVE INTEGRATED SILICON TRANSCEIVER DESIGN FOR HIGH DATA RATE COMMUNICATIONS

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With the explosion of information hungry computational and multimedia applications, the need for exceptionally high communication data rates has leapt to the forefront of electronic design. Advances is silicon technologies, manifested both in the speed of the transistors and complexity of the IC wiring stack, has bolstered the ability to meet new communication needs on a platform common to most consumer electronics. This ability becomes beneficial to historical approaches, both in system performance and costs, with the later being a huge benefit over existing solutions.

In this work the design of high speed wireless and wired communications on silicon platforms is investigated. The work uses both standard silicon CMOS technologies and silicon germanium BiCMOS technologies to demonstrate operations beyond 100 GHz and 100 GB/s. Activities in the wireless domain investigate both receivers and transmitters up to 100 GHz, with the most substantial work performed on the design and analysis of voltage controlled oscillators and low noise amplifiers. Differential and quadrature VCOs have been designed for operation between 16-64 GHz, with innovation in design methodologies and varactor degeneration. LNA design has been performed for operation from 20-110 GHz, with emphasis on balanced/unbalanced operations. Wireline development has focused on the design of two parallel systems for operation beyond 80 GB/s and 120 GB/s. Parallel development of half-rate 4 to 1 multiplexers and 1 to 4 demultiplexers has been

performed, as well as development of a 60 GB/s full rate flip-flop and 60 GHz static divider. Aggressive clocking techniques were developed to enable broadband operation from below 1 GB/s to the upper frequency bounds, and an area-centric design methodology was developed to mitigate the common perils of high frequency design.

Collectively, the circuits demonstrated here show a methodology aimed at enabling high frequency design despite the hurdles inherent in silicon processes. Most of these techniques are aimed at combating the limitations of the silicon substrate, even beyond the frequency limitations of the devices, and towards overcoming the amplified effects of interchip wiring at increased frequencies. In many instances the latter effects drive the electrical design of the circuits, where certain conventional techniques for high frequency design become impaired and undesirable.

# BIOGRAPHICAL SKETCH

Brian Welch was born August 7, 1979 in Schenectady, New York to Michael and Anne Welch. He grew up in Glenville, New York with brothers Sean, David, and Evan. Brian attended high school at the National Sports Academy in Lake Placid, New York, graduating in 1997. From August 1997 - May 2000 Brian attended Saint Lawrence University in Canton, New York and from August 2000 – May 2002 he attended Clarkson University in Potsdam, New York. In 2002 Brian received a Bachelor of Science in Physics and a Bachelor of Science in Electrical Engineering from the two schools, respectively. Beginning in August 2002 Brian continued his studies at Cornell University in Ithaca New York, receiving a Masters of Engineering degree in Electrical and Computer Engineering in May 2003, a Masters of Science degree in Electrical and Computer Engineering in August 2005, and a PhD in Electrical and Computer Engineering with a minor in Earth and Atmospheric Sciences in June 2006. During his education, Brian spent a year working with the ASIC Image/Package development group with IBM microelectronics in Burlington, Vermont, and another year performing research with the communications department at IBM's Thomas J. Watson Research Center. In 2004 Brian was the recipient of a Qualcomm design fellowship.

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# Chapter 1 Introduction

## *1.1 Motivation*

With the increasing ability for electronic processing of large volumes of information comes a growing need for communication systems capable of satiating this hunger. Three media have arisen to accommodate these needs, those being wireless, wired and optical communications. Between these platforms the differences lie in the communication medium and the systems necessary to harness that medium, and there differing benefits can be compared regarding performance, cost, distance, portability, power consumption, and more. While they each occupy certain arenas of the communication world, and each posses certain benefits over the other, they are similar in that they are in constant pursuit of higher data rates.

Historically high data rate communications have only been possible using III-V compound semiconductor materials such as Gallium Arsenide of Indium Phosphide [1]. This disparity in platforms from the computational workhorse of silicon has been a tremendous impediment to ubiquitous proliferation of these communication abilities. Beyond the complexity introduced by the requirement to employ a multi-platform system, these substrates have also typically far exceeded silicon technologies regarding cost, causing a major impediment to their use, especially within commercial applications. Recent advances in silicon platforms, including the evolution of silicon germanium technologies, have significantly diminished the advantages that III-V platforms have long held for high-speed operations [2]. While the significant differences between the two platforms, at least as it concerns high-speed operation, has typically been measured by the differences in the device transit frequency ($f_t$) and maximum oscillation frequency ($f_{max}$), the peripheral improvements in silicon

processes as they have been driven by development of improved digital capabilities have actually introduced benefits to the silicon technologies and revealed limitations of the III-V platforms.

With the evolution or cellular technologies throughout the past two decades wireless communications have become an integral part of almost all daily operations. This medium is now thoroughly employed in almost all telecommunications, from mobile phones and internet applications to GPS and satellite tracking. Early efforts toward this growth typically employed III-V technologies, however this was quickly supplanted by silicon as evidenced by the expansion of the mobile phone market [3]. Despite these advances, the improvements in data rate have been slow arriving, with transfer rates of even the fastest wireless internet protocols measured in the tens of megabits per second. Recent adjustments in the U.S. frequency allocations, however, have opened up new spectral bandwidths for communication evolutions, introducing the possibility for wireless communications beyond tens of gigabits per second.

Wired communications, be they through electrical or optical medium, have been quicker to adopt silicon technologies, and due to the nature of the channel have typically had much higher data rates than contemporary wireless technologies. Their presence in the silicon world is do in large part to their more common use in computational systems, as they have been the preferred workhorse for long and short haul digital communications. While early efforts developed single channel solutions capable of up to 40 GB/s data rates, many later efforts have investigated multi-dimensional integration for high speed parallel rates. While this type of development does have certain benefits, largely in terms of a relaxation of the requirements of the wireline transceiver, it achieves them at the price of much greater system complexity. By employing microwave techniques to these digital circuits using the most advanced

silicon processes these data rates can be increased threefold or beyond, with single channels capable of accommodating better than 100 GB/s communications.

## 1.2 Wireless Communications

The idea of wireless communications first became a reality with Guglielmo Marconi in December 1901 when he transmitted the fist wireless communiqué across the Atlantic Ocean from Poldhu, Cornwall to St. Johns, Newfoundland [4]. While he was not the first to hypothesize the ability to communicate using electromagnetic waves, it was this demonstration that first convinced the world that wireless communications was a viable alternative to wired telegraphy, and for this work he was awarded the Nobel Prize in Physics in 1909.

Throughout the mid to late twentieth century applications for wireless communications expanded to supply the needs of various public and private sectors, however it's ability to supply high data rates to service a large number of users, civilian or otherwise, didn't start to be realized until 1979 with the introduction of the first cellular telephone service. While the prohibitive costs and minimal coverage of early systems limited use to well within bandwidth capabilities, expanding usage, due largely to diminishing costs, has made much more rigorous the demands on system bandwidth. This increased demand, as well as the individual demand to transfer more data, has led to innovation in wireless coding and network infrastructure design, however it is ultimately in competition with the available spectral bandwidth. State of the art cellular systems occupy no more than a few tens of megahertz of spectral bandwidth, however due to the high demand typically no more than a few tens of kilohertz are available to any given user.

By moving to larger frequency allocations, located higher in the spectrum, many of the limitations of contemporary systems can be overcome, albeit while

introducing new challenges. Frequency allocations of 5GHz, 10 GHz, and more are rapidly become available for civilian applications, and standard committees are already aggressively at work developing licensing protocol for their use. The three most promising bands are all within the millimeter-wave regime (mmWave), occupying the spectrum from 56-64 GHz, 71-76 & 81-86 GHz, and 92-100 GHz. Further bands exist beyond 100 GHz with even larger available frequency allocations, and it is anticipated the design techniques developed herin will be able to accommodate these future applications when future advances in silicon processes (namely transistor speed) enable their development.

Prior work in microwave and mmWave development has focused almost exclusively on III-V materials [5,6], with a few notable exceptions [7,8]. In this work we investigate the abilities to replace these circuits with silicon components, to realize certain benefits incumbent in the ability to design a completely integrated system, and to mitigate the costs of these applications to turn them into consumer reality. Much of the work towards these ends has been in the development of high speed voltage controlled oscillators (VCOs) and low noise amplifiers (LNAs) for receiver applications, however substantial efforts peripheral to this work have also been exerted toward developing both up and downconvert mixers, bandpass and lowpass filters, image reject filters & high power amplifiers, dynamic dividers, and numerous passive structures including transmission lines, pads, baluns, and power dividers.

## *1.3 Wireline Communications*

Shortfalls in the data transfer rates of wired communications have long been the bottleneck of computer development, with limitations arising shortly after the beginning of the proliferation of personal computers. While certain limitations have been attributed to the communication medium, namely the silicon platform, advances

to overcome these limitations have not mitigated their effects entirely. To the contrary, the problems introduced by long haul communications have often driven circuit complexity to become more sensitive to the perils of the silicon process, and while this complexity is often necessary it can be combated by applying mmWave techniques onto more advanced silicon processes. It is important to note that these communication limitations, especially as they concern the distances of the electrical links, are relatively independent on the behaviors of the silicon devices but depend predominately on the system wiring. Substantial efforts have been exerted to mitigate these effects, including the development of low permittivity, low loss insulators and high conductivity wiring (copper), however these changes only delay the inevitable bottleneck. To compliment these efforts and expand their usefulness the design techniques developed to enable better development of wireless systems have been employed to broadband wired systems.

## *1.4 Contributions to the Field*

The work presented herin contributes to the field of electronic communications by developing certain design techniques and methodologies for mmWave development, and employing them into high data rate circuit applications including the fastest reported silicon wireless amplifier and wireline multiplexer/demultiplexer (MUX/DEMUX). Vital to this work is the development of techniques which enable single substrate integration, where we are able to fully exploit the benefits of silicon by removing the design bottleneck present with interchip transitions. A number of new design techniques and inventions are presented for VCO development, most notably the introduction of variable capacitance emitter degeneration. LNA pursuits have compared the behaviors of SiGe HBT processes to standard Silicon CMOS processes, investigated the behaviors of single-ended to differential conversion, and studied

operations beyond 100 GHz. Investigation into high power circuits for applications within a wireless transmitter have also been performed, in the manner of a high power mmWave oscillator and mmWave transmitter.

Contributions to the wireline field can be seen through the bandwidth extension available using mmWave techniques, even while employing rather conventional design techniques. Within this work standard current-mode logic (CML) is employed, with novelty introduced in clocking and optimization. The circuits designed include a half-rate 4 to 1 MUX and 1 to 4 DEMUX, as well as a 60 GHz static divider and 60 GB/s full-rate flip-flop. The largest challenge in the design of these systems is providing a suitable clock across the entire operating bandwidth. Here significant efforts are placed at translating a sinusoidal clock input to a square wave across the wide range of input data rates. Another prevalent challenge in the design of these circuits is owed to the large bandwidth of the system, which introduces hurdles in damping of signal transitions. The large bandwidth is necessary to accommodate fast transitions in the data path, however it often introduces overshoot in slower transitions. Combating this problem, as well as damping clock feedthrough (especially at high data rates) is done by employing common mode loads, which are effective at detuning the resonance common in the high $f_t$ devices.

## *1.5 Chapters Overview*

In chapter 2 the limitations of mmWave design in a silicon technology are dissected. In chapters 3 and 4 VCO development is discussed through it's evolution towards higher and higher frequencies, covering the spectrum from 16 GHz to 64 GHz. Early discussions focus on the movement from standard LC type tanks to microwave type resonators, with later chapters discussing the electrical compromises and design techniques necessary to achieve high frequency operation through the

mitigation of unwanted parasitics. Chapters 5 and 6 discuss the development of LNAs from 20 GHz to 94 GHz, and again outlines the evolution of design abilities to push the limits of silicon technologies. In both of these pursuits the challenges of the design are most evidently realized through the operation frequency of the circuits relative to the technology capabilities, with early works performed using significantly lower $f_t$ technologies. Chapters 7 and 8 discuss wireline operations, especially as design diligence and optimization supplants high risk electrical designs to achieve high frequency operations. Chapter 9 recaps the techniques developed and their application to all platforms for high data rate communications, and proposes some future uses to further expand silicon capabilities.

# Chapter 2 Challenges of mmWave Silicon Design

The challenges inherent in the design of mmWave systems using silicon technologies can be dissected into three distinct parts: Limitations of the silicon devices and front end of the line, limitations of silicon wiring and back end of the line, and limitations in IC packaging. While the advancement of silicon devices is beyond the scope of this research, its ability to mandate certain electrical compromises is one of the most underlying themes to this research. Likewise are the electrical compromises required due to the limitations of the silicon back end, especially as it concerns mitigation of parasitics (especially unmodeled parasitics). The packaging issues are addressed through the improvement in abilities to integrate components within a single silicon IC, eliminating the need for many connections between an IC and its package, thereby overcoming the hurdles incumbent in doing so.

## *2.1 Front End of the Line Design Hurdles*

Conventional wisdom suggests that the most fundamental limitation of any technology, at least as it regards the operation frequency of the system, is the transistors maximum transition frequency ($f_t$) and maximum oscillation frequency ($f_{max}$). While this holds true for certain frequencies of operation, its validity has become more suspect in recent years. Despite increased advances of transistor frequencies into the hundreds of gigahertz, operational frequencies of systems employing these technologies have not kept up. While in the large scale digital sense other factors may influence the operation of these systems (namely power consumption and heat dissipation), in the communications regime there are other forces at work inhibiting the potential of modern silicon technologies.

One concept missing from the improvement in the frequency response of a particular device is how it affects the frequency response of a particular system. The underlying difference between the two ideas is that the limiting factor on the ability of a system to operate under high frequency isn't the $f_t$ or $f_{max}$ of the device, but other elements within the system. These elements, at least as they are examined within this work, are the loss and parasitic elements of the transistor, and the effects that those exact upon the system. Until recently the abilities of the components of a silicon technology peripheral to the devices were far from the limiting factor in the design, so improvements in device technologies scaled directly to improvements in performance. This assumed, among other things, that the ability to provide gain at certain frequencies was the only limitations of the devices, and that the impedances that characterize the termination characteristics of a device were of little consequence. It is for that reason that many techniques aimed at extending the bandwidth of a circuit through the use of more active devices were developed, because these devices were seen as being largely transparent to the load impedance of whatever node they connected to. High frequency design however, at least at it is defined here, is described as the operation regime where this assumption no longer holds true, and every device acts to restrict the bandwidth of the system.

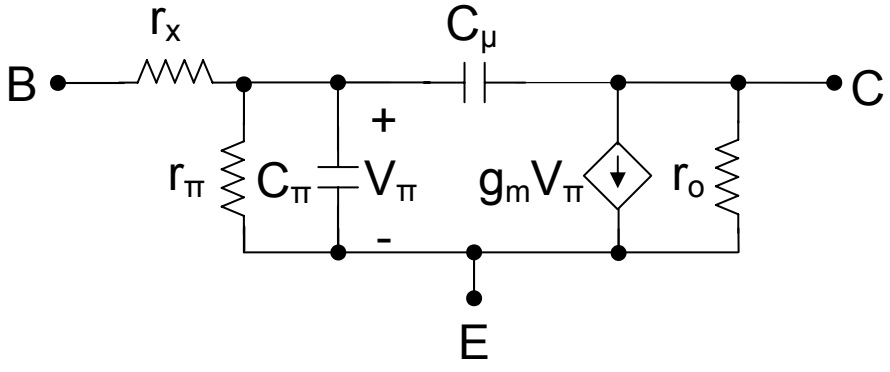



Figure 2.1: BJT Small Signal Model

A simple model of the BJT with parasitic capacitances labeled can be seen in Figure 2.1, where the two AC components are the capacitors $C_\pi$ and $C_\mu$. For the conventional wisdom of high frequency design to apply, these capacitances must scale (inversely) with frequency. Deconstructing the capacitances into their components the capacitance $C_\pi$ can be constructed from the base diffusion capacitance and base-emitter depletion capacitance, and the capacitance $C_\mu$ can be constructed from the collector-base depletion capacitance [9]. The diffusion capacitance at the base junction can be represented as:

$$C_{de} = \tau_f \frac{di_C}{dv_{BE}} \tag{2.1.1}$$

Where $\tau_f$ is the forward base transit time. While $\tau_f$ is expected to scale with $f_t$ (since $f_t$ is determined by the electron field velocity across the base), $di_C/dv_{BE}$ may not. Assuming that $\tau_f$ scales with frequency it would be expected that if $di_C/dv_{BE}$ remained constant the capacitance would scale, however $di_C/dv_{BE}$ may increase with frequency. This is true because high $f_t$ devices typically have higher current densities than low $f_t$ devices, meanwhile the bias voltages for the devices as scaled lower to prevent junction breakdown. Assuming these higher current densities for lower voltage swings the second quantity can instead increase with frequency, negating the decrease of $\tau_f$ and preventing the diffusion capacitance from scaling linearly.

Another component of the capacitance $C_\mu$ is the depletion capacitance of the base-emitter junction, $C_{je}$. This is also the main component of the capacitance $C_\pi$, only across the collector-base junction. This capacitance arises from the charge storage characteristics of a reverse biased p-n junction, where the total amount of charge stored in the junction is dependent upon the bias voltage across the junction.

Characteristic of this behavior is the depletion depth, which has the following dependency on the voltage across the reverse biased junction [10]:

$$x_d = x_n + x_p = \sqrt{\frac{2\varepsilon(V_{bi} - V)}{qN_D(1 + N_D / N_A)}} + \sqrt{\frac{2\varepsilon(V_{bi} - V)}{qN_A(1 + N_A / N_D)}} \tag{2.1.2}$$

Where ε is the dielectric permittivity of Silicon, $N_A$ and $N_D$ are the acceptor and donor concentrations, respectively, V is the voltage applied to the pn junction and $V_{bi}$ is the built in voltage of the junction. From this the depletion capacitance across the junction can be written as:

$$C = \varepsilon S / x_d = S\sqrt{\frac{q\varepsilon\left(\sqrt{N_D(1 + N_D / N_A)} + \sqrt{N_A(1 + N_A / N_D)}\right)^2}{2(V_{bi} - V)}} \tag{2.1.3}$$

Where S is the cross sectional area of the junction. From this equation it can be seen that major factor in the depletion capacitance of a transistor is the area of the depletion region, which is dependent upon the area of the device. While traditional advancements in device $f_t$ were achieved through scaling of the device area, contemporary devices employ additional methods, causing $f_t$ to scale much more rapidly than the device area. While variations of the other parameters (permittivity and acceptor/donor concentrations) might occur through the novel doping employed in high speed devices, it is not enough to compensate the effects of the transistor area, and as such the depletion capacitance does not scale with $f_t$.

Another limitation with high $f_t$ devices owes to the fact that these capacitances are bias dependent. Since small signal operation and modeling requires that a device behave consistently over a small range of powers, one can conclude that for this to be

true the effects of the changing capacitance across these powers must be negligible. While this is certainly true for the cases where the device capacitance is a relatively small part of the load impedance at a particular node, at higher frequencies as this device capacitance becomes a greater portion of the entire capacitance at a given node the systems tolerance to variations in these parameters diminishes, hence undermining the validity of small signal operation. Without careful design practices this limits the ability of a system to operate correctly over a large dynamic range, and can lead to greater variations in system performance due to transistor heating and process variations.

## 2.2 Back End of the Line Design Hurdles

While device capacitances play an ever increasing role in the effect of high frequency designs, so to do the parasitic natures of Back End of the Line (BEOL) components. Beyond the limitations that known parasitics place on a system, high frequency design is often saddled with the additional burden of inexact parasitic extraction. This inability to accurately model certain components leads to increased variability in high frequency designs, variability that can cause large deviations in system operation.

The most frequently used BEOL components in silicon design are wires, capacitors, bondpads, and transmission lines. Within the context of this work wires are described to be any piece of metal used to distribute a signal or power without the closely controlled environment of a transmission line. This typically includes any wiring on the metal layers nearest the substrate and often includes wiring amongst active devices & resistors, and also includes vias. While capacitors often have an associated model one limitation to their use (in certain parts of a circuit) is the introduction of wiring to accommodate their large size. Another BEOL element that

introduces limitations dues largely to its size is a Bondpad, which typically must be quite large to accommodate packaging or probing. This large size causes the pads to be highly capacitive, restricting the bandwidth of the nodes they employed. The most reliable element in the BEOL design is generally transmission lines implemented on the top few metal layers. Their well defined environment removes many modeling uncertainties and they are easy to manipulate to achieve optimal layout geometries. At high frequencies they are often preferred to inductors for resonant structures due to their well defined, and low loss, return paths.

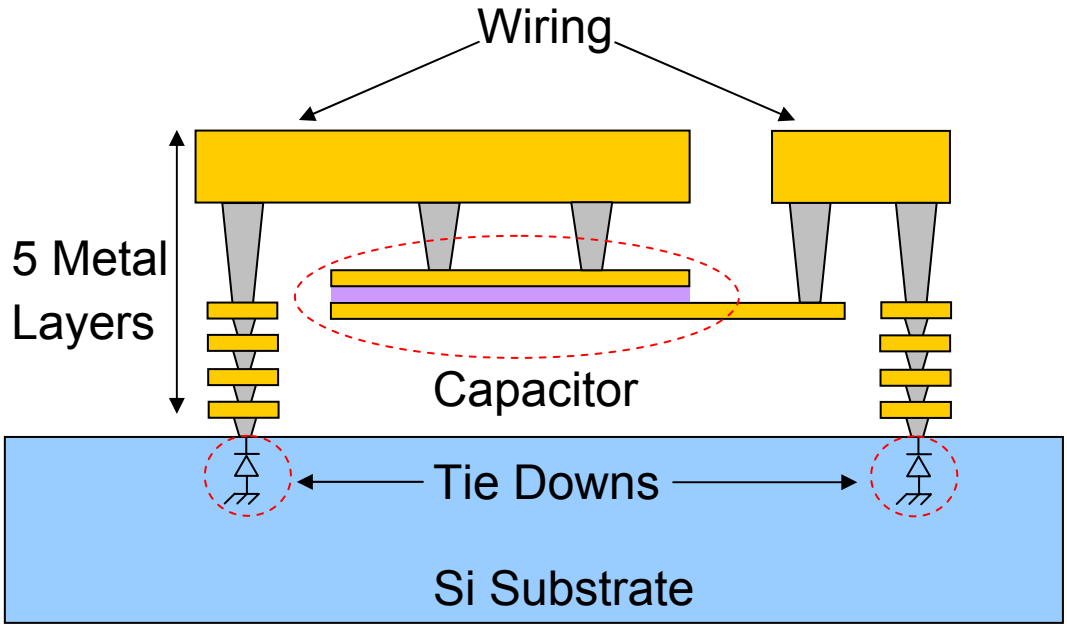



Figure 2.2: Metal-Insulator-Metal (MIM) Tie Down with Wiring

In Figure 2.2 a Metal-Insulator-Metal (MIM) capacitor can be seen [11]. Accompanying the capacitor is the minimum amount of wiring necessary to its implementation, as per the frequently mandated capacitor design rules for ESD compliance. Note that for both the top and bottom metal layers of the MIM capacitor, the circuit must be tied down to the substrate through the highest metal layer. In doing so a significant amount of wiring is needed, often increasing the size of a capacitor by up to 50%. Given that the minimum size available for most capacitors is around 10 μm by 10 μm, the smallest realistic capacitor cell is about 15 μm by 15 μm. Beyond the limitations inherent in the wiring necessary for the capacitor comes the large parasitic capacitance the capacitor has to ground, which restricts its use to nodes that aren't tremendously sensitive to excess shunt capacitance (namely, matched 50 ohm loads and not intracircuit high impedance nodes, such as a VCO tank). Also, considering that the size of the active devices used at mmWave frequencies are minimized to combat the capacitive effects discussed in the previous section, and often occupy no more than a few square microns, introducing capacitors to a circuit can easily increase the effective active area by several thousand percent, greatly increasing variability in the design. With these effects in mind the designs described in the following chapters are devoid of capacitors wherever necessary, with greater emphasis placed on those circuits operating at the highest frequencies (this can be seen in the transition from AC cross coupled VCOs at 20 GHz to DC cross coupled VCOs at 60 GHz).

Similar to the limitations of unmodeled wiring and unnecessary capacitors severe limitations are placed on a design due to the parasitic behaviors of bondpads necessary for inter-chip communication. Due to limitations in the ability to package and probe an IC bondpads need to be exceptionally large compared to other structures, which makes them an incredibly capacitive element. While this capacitance has little

effect at low frequencies at millimeter wave (mmWave) frequencies a pad can be far from electrically transparent.

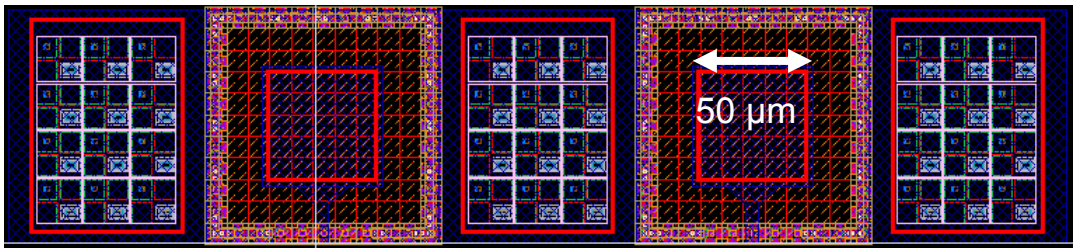



Figure 2.3: 100 µm Pitch GSGSG Pad Array with 50 µm x 50 µm Signal Pad

An advanced mmWave IC bondpad can be seen in Figure 2.3, with a plane on the top metal layer shielded from the substrate with a metal backplane. Bondpads necessary for mmWave applications range in size from a minimum of 50 µm by 50 µm (minimum size possible to probe) to over 100 µm by 100 µm (for ribbon bond applications), and can employ metal backplanes, polysilicon backplanes, or deep trench $SiO_2$ isolation lattices. While great lengths are taken throughout this work to minimize the effects of pads on IC performance, even with the optimal pad (minimum sized with a metal backplane) severe bandwidth limitations are placed on any node connected to a pad, even without accounting for the effects of the interconnect beyond the pad (solder-ball, ribbon bond, bond wire). While this may seem a great hurdle to mmWave design, it is actually a great benefit to silicon mmWave design because the ability for large scale integration prevents the use of many pad bearing high frequency nodes.

With these limitations considered, it becomes advantageous to employ transmission lines wherever possible in BEOL design. Even with their employment certain geometrical constraints may introduce excessive wiring, although that can be

minimized through careful design. As will be demonstrated in the works that follow, as it relates both to transmission line deployment and electrical design practices, the most important design practice is not to achieve the optimal performance but the most reliable. This realization demonstrates the fact that certain electrical designs and physical geometries will introduce more unknowns to the circuits than others, with the tolerances for unknowns within mmWave circuits being exceptionally small.

## 2.3 Package Design Hurdles

While largely outside the scope of this work, the ability to package mmWave silicon elements requires some mention. While the difficulties in transitioning between silicon and package substrates was mentioned in the scope of bondpad design, further limitations are inherent in packaging abilities that mandate the increased integration of mmWave silicon electronics. To accommodate the high frequencies capable with mmWave silicon design comparably advanced packaging technologies are necessary, although always at a highly elevated cost. By integrating more functionality on a single carrier fewer high speed interconnects are necessary through the packaging, which (when properly done) can allow for the dramatic reduction in package and therefore module costs.

Also limiting in packaging of these elements are the inconsistencies of the interconnects between the IC and the package, and variations in package characteristics. While the later is largely due to variations in the flip-chip, ribbon-bond, or wire-bond interconnect, it can also be caused by variations in encapsulation materials and package alignment. Variations in package characteristics can also be caused by variations in encapsulation and package geometries, further underscoring the benefits of increased silicon integration.

## 2.4 Silicon Advantages

While III-V semiconductors have advantages both in their higher ft and the low parasitic nature of their semi-insulating substrate, they are handicapped by their inability to be readily integrated without packaging multiple modules, and by their limited abilities for system complexity and integration with their simple BEOLs. With these differences considered, the improvements in silicon transistor speed have opened new doors due largely to its ability to achieve high levels of single IC system integration with electrically simple circuits. In doing so many of the elements which can restrict the bandwidth of the system or reduce it's tolerance to process and performance variations are eliminated, and the likelihood of success, especially success without multiple design cycles, is dramatically increased.

Fundamental to overcoming the limitations of silicon is the ability to design highly accurate circuits with largely inaccurate extraction and simulation tools. While this hurdle is not exclusive to silicon technologies, the low integration levels of III-V circuits allows for alternative modeling methodologies (field solver vs. electrical extraction), that have prevented the need of the solutions described herin until this time. The ultimate goal with these design methodologies is to eliminate elements susceptible to modeling inaccuracy wherever possible, and instead employ more robust circuit elements (most often transistors and transmission lines). One example of this, as previously stated, is the limitation in employing BEOL capacitors due to the large amount of wiring necessary for their accommodation. Outlined in the following chapters are families of wireless and wireline circuits designed to demonstrate these techniques, with ultimate performance achieved at frequencies at or above any other silicon IC design to date.

# Chapter 3 VCO Design and Innovation

## *3.1 VCO Fundamentals*

Voltage controlled oscillators and local oscillators are employed in many computational applications today. While the basic VCO is a relatively small component of the larger circuits it typically contributes to, including Phase Locked Loops and Frequency Synthesizers, it is often the limiting factor on system performance. A simple oscillator can be created with the negative feedback system as shown in Figure 3.1. [12].

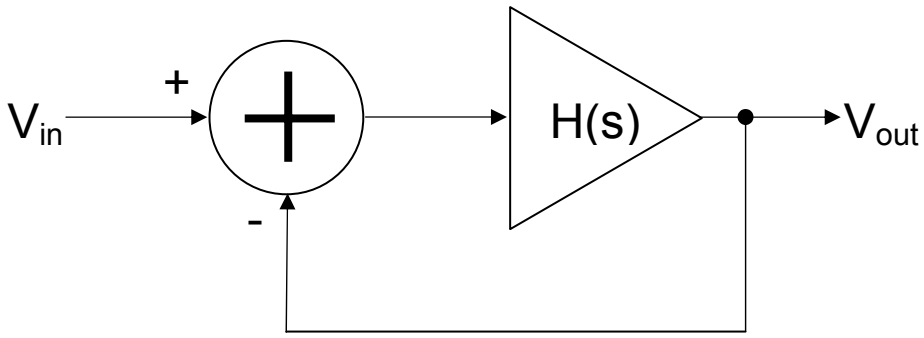



Figure 3.1: Oscillator created through negative feedback

In Figure 3.1 the transfer function can be written:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 - H(s)} \tag{3.1.1}$$

In this system for oscillation to occur H(s) = +1, which describes the situation where the closed loop gain approaches infinity giving rise to an oscillations at frequency $\omega_0$. Equation 3.1.1 can also be written as:

$$|H(s)| = 1 \tag{3.1.2}$$

$$\angle H(s) = 180° \tag{3.1.3}$$

Equations 3.1.2 and 3.1.3 are also called Barkhausen's criteria, and can be applied to any feedback system, and are not restricted to that displayed in Figure 3.1. These equations describe a system where the feedback loop suffers no losses, and the signal returned about the feedback path is out of phase with the input signal. Other conditions, where the signal returns in phase with the input can cause stable conditions (i.e., latch up), or if the returned is imbued with only a minor phase shift from the input signal then oscillation might require greater loop gain (to compensate losses due to destructive interference).

Another model for the oscillator, and one which we will apply to our design examples herin, introduces a resonant circuit to transform Figure 3.1 into a one-port network as shown in Figure 3.2.

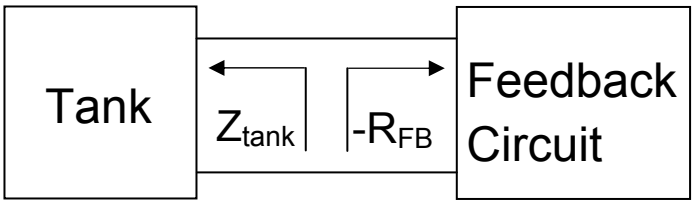



Figure 3.2:: A one port resonant type oscillator

In practice most VCOs for high frequency applications employ a circuit similar to that in Figure 3.2 to achieve oscillation. In the ideal case this oscillation within the resonant tank would be self sustaining assuming some initial excitation, but as any resonant tank is composed of some loss mechanisms additional circuitry must be provided to contribute continued excitation. The loss mechanisms within the tank can be seen in Figure 3.3 (a), with an equivalent circuit shown in Figure 3.3(b) to represent the losses as a single parallel element Rp. To compensate the tank losses attributed to

$R_p$ the feedback circuit of the oscillator is often considered to act as a negative resistance, where the negative resistance ($-R_{FB}$) of the circuit must be equal to (or greater than) the losses in the tank to sustain oscillation. It is in the design of the tank to mitigate loss mechanisms, and the ability to design circuits capable of high frequency excitation that the challenges faced in these design exercises is presented.

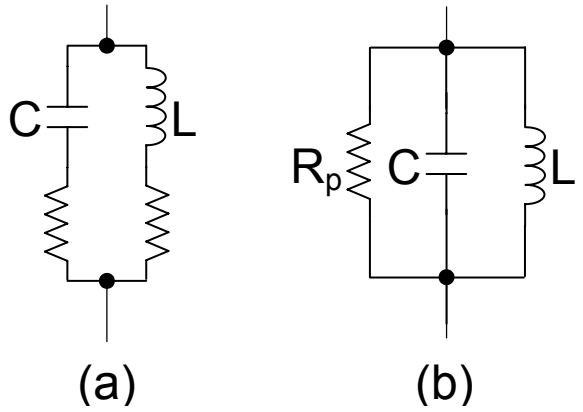



Figure 3.3: (a) LC resonator with parasitic losses, (b) equivalent circuit

With all oscillators the primary metrics of performance are the circuit's oscillation frequency, phase noise, tuning range, output power, and power consumption. Other concerns in oscillator design, especially as they are applied to a VCO's placement in PLLs and other circuit, are tuning gain and supply sensitivity. Typically the limiting factor in VCO design is the circuit phase noise, and it generally competes with the other primary metrics of system performance. As proposed by Leeson the phase noise of a VCO can be derived from Equation 3.1.4 [13].

$$PN(\Delta f) = kTR_p \frac{F}{V_o^2}\left(\frac{f_{OSC}}{Q\Delta f}\right)^2 \tag{3.1.4}$$

Where k is Boltzmann's constant, T the absolute temperature of the system, $R_p$ the parallel tank resistance (as shown in Figure 3.3(b)), F is the noise factor of the system, $V_o$ is the oscillation amplitude, and Q is the quality factor of the tank.

In high frequency operations it is the tank quality that is typically the limiting factor in oscillator design, and the effect that links the previous design metrics. The quality factor of a tank is described as the energy stored in the tank to the energy lost with each cycle, and as such is dependent upon the losses in the tank [14]. The effect of this can be seen by comparing the two spectrums show in Figure 3.4.

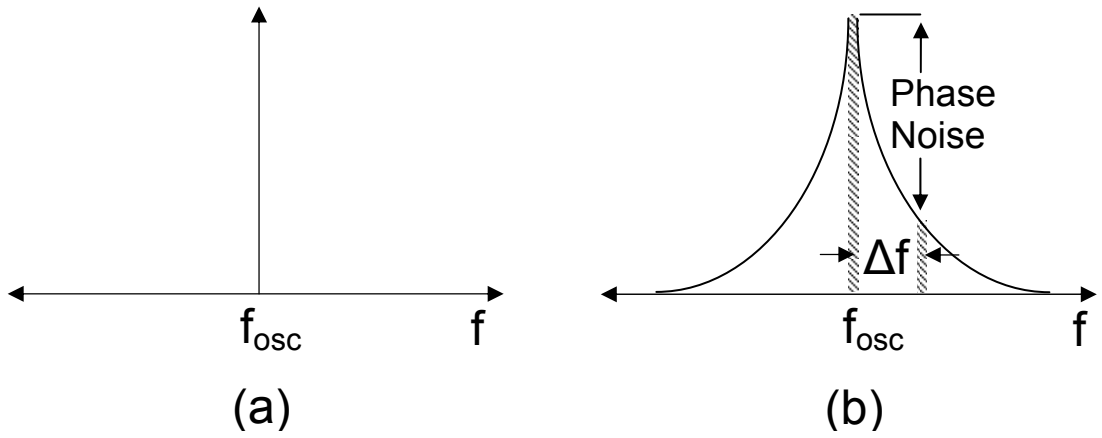



Figure 3.4: Output spectrum of an ideal oscillator (a) and actual oscillator (b)

The quality of the two elements of the tank can be written as:

$$Q = \frac{L\omega}{R_s} \tag{3.1.5}$$

$$Q = \frac{1}{\omega C R_s} \tag{3.1.6}$$

Where $R_s$ is the series resistance of the respective component. Typically, the quality factor of the inductor employed in the tank is the limiting factor of the VCO, however the capacitor can have a significant impact on tank losses. While the finite quality of the capacitors can have an impact on the phase noise of the circuit, even absent these effects the capacitor can lead to degradation of the oscillator. Consider that the oscillation frequency of the tank is:

$$\omega = \frac{1}{\sqrt{LC}} \tag{3.1.7}$$

The quality factor of the tank at resonance can then be found to be:

$$Q = \frac{1}{R_P}\sqrt{\frac{L}{C}} \tag{3.1.8}$$

Where $R_P$ is the parallel tank resistance as shown in Figure 3.3 (b). This equivalent resistance can be found by equating the parallel and series forms of both the RL and RC networks as shown in Figure 3.5, where the resistance $R_p$ is the parallel product of the losses of the two elements.

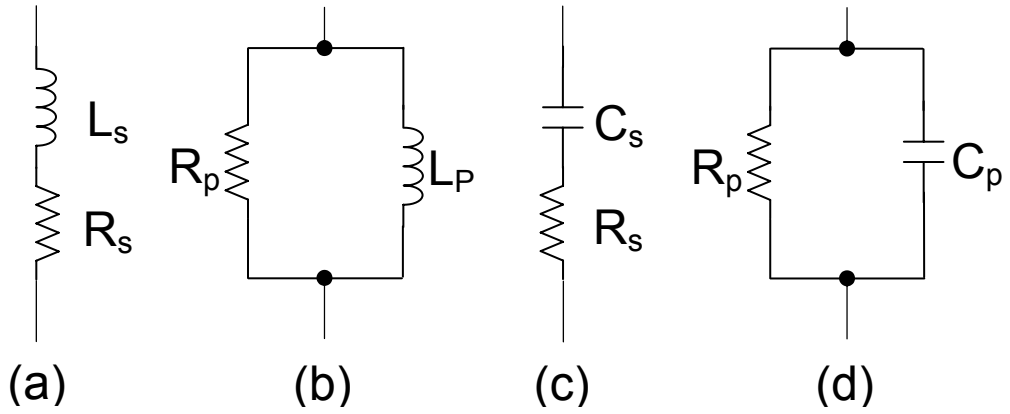



Figure 3.5: Series and parallel equivalent circuits of (a) & (b) an inductor and (c) & (d) a capacitor.

From the circuits shown in Figure 2.5 the following equations can be written for the non-ideal inductor and capacitor, respectively:

$$j\omega L_s + R_s = \frac{j\omega R_P L_p}{R_P + j\omega L_P} \tag{3.1.9}$$

$$\frac{1}{j\omega C_S} + R_s = \frac{1}{j\omega C_P}\frac{R_P}{R_P + 1/j\omega C_P} = \frac{R_P}{j\omega C_P R_P + 1} \tag{3.1.10}$$

These equations can be rewritten as:

$$-\omega^2 L_s L_P + j\omega\left(L_s R_P + L_P R_S\right) + R_S R_P = j\omega L_P R_P \tag{3.1.11}$$

$$-\omega^2\left(C_S C_P R_S R_P\right) + j\omega\left(C_s R_s + C_P R_P\right) + 1 = j\omega C_s R_P \tag{3.1.12}$$

Solving for equivalent parallel inductance and resistance values yields:

$$L_s R_P + L_P R_s = R_P L_P \tag{3.1.13}$$

$$R_s R_P - \omega^2 L_s L_P = 0 \tag{3.1.14}$$

Combining and solving to get:

$$L_P \approx L_s \tag{3.1.15}$$

$$R_P \approx \frac{{L_s}^2 \omega^2}{R_s} = Q^2 R_s \tag{3.1.16}$$

Likewise, solving for the equivalent parallel capacitance and resistance yields:

$$C_s R_s + C_P R_P = C_s R_P \tag{3.1.17}$$

$$-\omega^2 C_s C_P R_s R_P = 0 \tag{3.1.18}$$

Combining and solving to get:

$$C_P = \frac{C_s}{1 + \omega^2 {C_s}^2 {R_s}^2} \approx C_s \tag{3.1.19}$$

$$R_P = R_s + \frac{1}{\omega^2 {C_s}^2 R_s} = R_s + Q^2 R_s \tag{3.1.20}$$

In both equations 3.1.16 and 3.1.20 the parallel resistance goes roughly as the square of the quality of the element (with an additional constant, Rs added in the case of the capacitor). In each case the quality is dependent on the inverse of the series resistance, so minimizing the series losses of the individual components increases the parallel resistance of the tank (decreasing the equivalent tank losses), thereby increasing the overall quality of the tank. In most cases the capacitor losses are quite small, so the limiting factor on the tank quality is the quality of the inductor.

From the result of equation 3.1.7, it can be seen that given a larger capacitance the oscillation frequency can only be increased by decreasing the inductance. Since most VCOs employ varactors to allow for variations in capacitance in the tank, a larger capacitance is often employed to allow for a larger tuning range (as the variations in the capacitance are due to the size of the capacitor). Since doing so mandates the use of a smaller inductor to maintain the same oscillation frequency, which, independent of changes in resistance leads to a lower tank quality (equation 3.1.16), the increase in tuning range of the VCO typically increases the phase noise of the circuit. Beyond this, larger capacitors also are more susceptible to noise on the tank and bias nodes, which can lead to instantaneous variations in capacitance and introduce further noise mechanisms into the system.

Leeson's equation demonstrates that by increasing the oscillation amplitude at the tank the phase noise of the circuit can be improved, as it is proportional to the reciprocal of the oscillation amplitude squared. Often, however, increasing the oscillation amplitude is not readily achievable without increasing the device size in the feedback path, to drive more current across the LC tank. Increasing that device size, however, often subjects the circuits to more noise contributions, especially the classical noise mechanisms of a transistor as seen in Figure 3.6 and described in equations 3.1.21-3.1.23 [15].

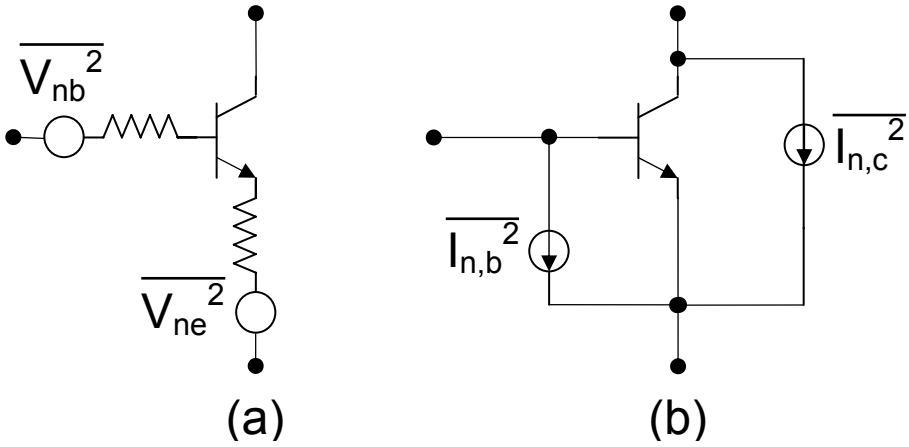



Figure 3.6: Transistor (a) Thermal noise and (b) shot noise

$$\overline{V_n^2} = 4kTR\Delta f \ , \ \overline{I_n^2} = 4kT\left(\frac{2}{3}g_m\right) \tag{3.1.21}$$

$$\overline{I_n^2} = 2qI \tag{3.1.22}$$

$$\overline{V_n^2} = \frac{K}{WLC_{ox}}\frac{1}{f} \tag{3.1.23}$$

Equations 3.1.21 are the thermal noise expression for BJT and MOS type devices, where the expression $\overline{V_n^2}$ represents the series voltage noise sources as they may exist in the base and emitter of the device, and expression $\overline{I_n^2}$ is the equivalent parallel noise source for MOS transistors, as it exists between the source and drain of the device. Equation 3.1.22 is the equivalent expression for the shot noise in the device, which is a Gaussian process dependent upon the transfer of charge across an energy barrier. Equation 3.1.23 is the flicker noise also inherent in MOS devices, and is a gate connected source which represents noise due to the random trapping of charges at the silicon dioxide-silicon interface.

These noise sources are detrimental to the oscillator primarily due to the variations in capacitance they can incur upon the varactors. The random fluctuations of the bias voltage across the varactors causes spreading in the VCO spectrum, and

these fluctuations are more pronounced with larger devices consuming more current. Also problematic with larger devices is the parasitic capacitance introduced upon the tank by the collector (or drain for the case of MOSFETs) load, which pulls down the oscillation frequency (and thereby mandates a smaller inductive load) in a similar manner as an increased varactor size does.

## 3.2 Fundamentals of the Resonant VCO

The work described herin employ exclusively resonant type VCOs for frequency generation. It is primarily the oscillation frequency that dictates the need to employ resonant type oscillators, as the oscillation frequency is not limited by the switching time of a logical gate but instead determined by the resonant frequency of the tank. That being said, the bandwidth of the circuit is still limited by the speed of the devices, as they are required to inject energy at the oscillation frequency to sustain VCO operation. A simplified version of a resonant type oscillator (with an Inductor/Capacitor based tank) can be seen in Figure 3.7 (a) [12]:

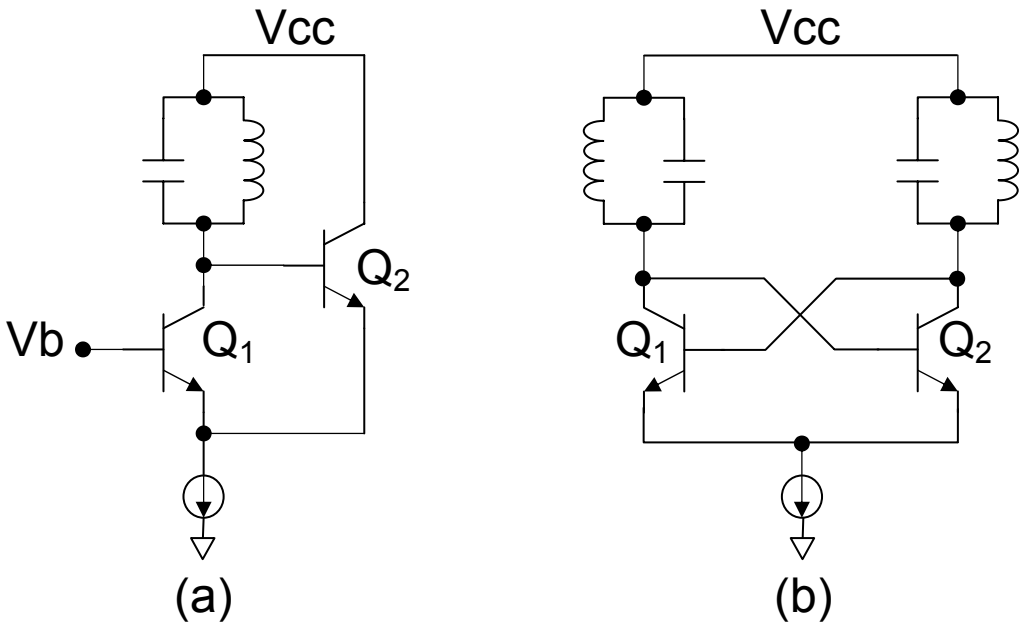



Figure 3.7: (a) Simplified resonant type VCO with emitter-follower feedback, (b) Simplified symmetrical resonant type VCO with cross-coupled pair.

In Figure 3.7 (a) transistor $Q_1$ sources energy into the LC tank, and transistor $Q_2$ acts as the feedback loop to inject the signal into the emitter of $Q_1$. The base of transistor $Q_1$ is biased at a fixed DC voltage, typically equivalent to Vcc. Here the bias current through $Q_1$ and $Q_2$ is set by the current source shown connected to the emitter of the two devices. In Figure 3.7 (b) an additional LC tank is introduced to the collector of transistor $Q_2$, with feedback provided by applying this collector voltage of $Q_2$ to the base of transistor $Q_1$.

By changing the circuit to that shown in Figure 3.7 (b), a few things can be achieved. Foremost, unlike the circuit in Figure 3.7 (a) differential outputs are available with the symmetrical model, which is a large benefit in silicon IC development. Also, as the two transistors are coupled at the emitters, some common

mode rejection is achieved which can inhibit even order harmonic products. One potential drawback of the circuit in Figure 3.7(b) is the presence of a second inductor, which could complicate the layout of this circuit (which can be relieved by using symmetrical, center tapped inductors). Another drawback of this circuit is the additional noise that may be introduced by the second tank, specifically the noise mechanisms within the second varactor.

## 3.3 Capacitive Degenerated Voltage Controlled Oscillators

A recent innovation that expands upon the abilities of the negative resistance type oscillator described in the previous section is the introduction of capacitive degeneration into the feedback loop of the system. Capacitive degeneration has long been a useful modification on linear circuits [16], however it wasn't until recently that this technique was first applied to oscillators [17]. Reviewing the work from [17] modifications to the typical negative resistance type resonant oscillator can be seen in comparison of Figures 3.8 (a) and (b).

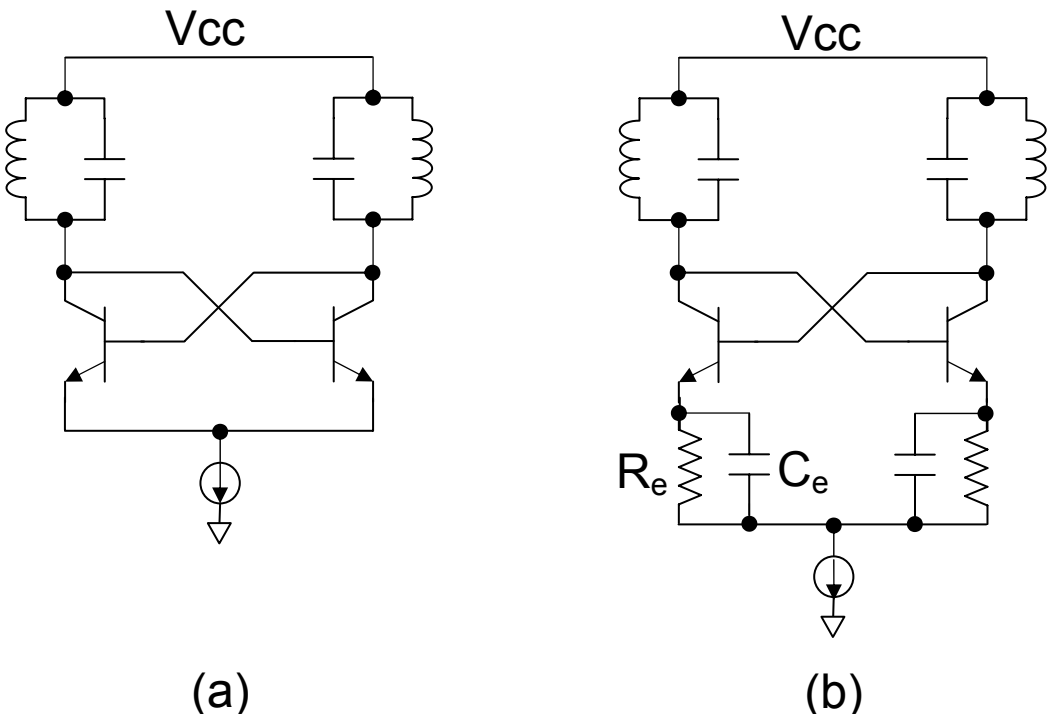



Figure 3.8: (a) Traditional negative resistance type resonant oscillator and (b) capacitive degenerated resonant type oscillator.

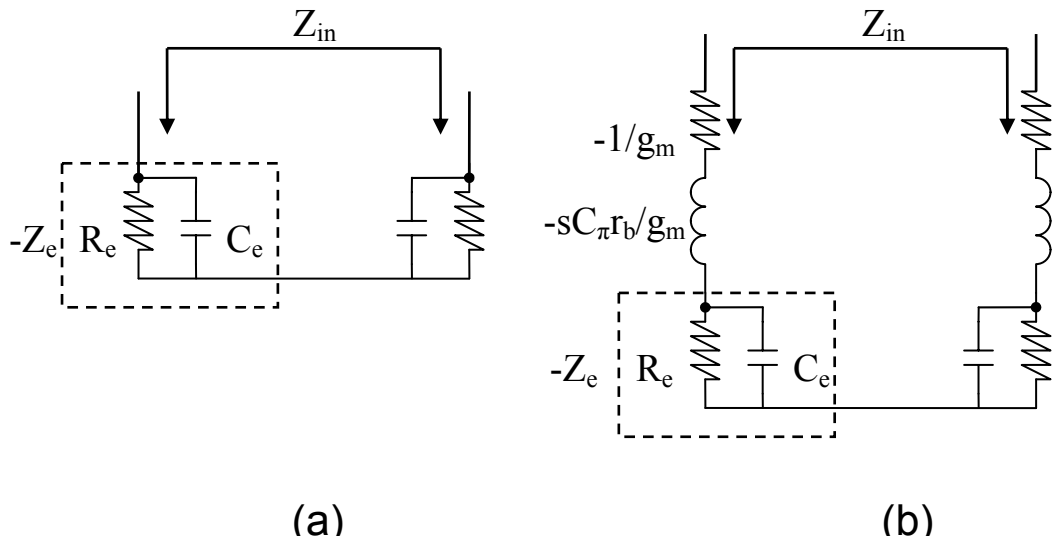



Figure 3.9: Emitter degeneration equivalent circuits for (a) first order and (b) realistic cases.

In Figure 3.8 (b) the parallel pair of $R_e$ and $C_e$ are added to the emitters of each half of the cross-coupled pair, the primary element being the degeneration capacitors. From Figure 3.9 (a) the first order effect of these elements is to introduce a negative capacitance at the collectors of the two devices composing the cross-coupled pair. This negative capacitance has the effect of moving the pole at the collector higher in frequency by cancelling out some of the capacitive load on the node. Modifying equation 3.1.7 to reflect the introduction of the capacitors a simple expression for the oscillation frequency becomes:

$$\omega = \frac{1}{\sqrt{L(C - C_e)}} \tag{3.3.1}$$

Equation 3.3.1 oversimplifies the behaviors of the cross coupled pair, however, and instead gives an ideal representation of the oscillation frequency with the introduction of degeneration capacitors. Realistically the oscillation frequency will be less than that given by Equation 3.3.1, as mandated by both the non-idealities of the negative resistance circuit and other parasitic elements which constitute the oscillator, as shown in Figure 3.3.2 (b). From Figure 3.3.2 (b) the following design equations can be derived to describe the behavior of the non-ideal VCO:

$$R > R_{EE} + \frac{{X_{EE}}^2}{R_{EE}} \tag{3.3.2}$$

$$X_{EE} = \frac{\left({R_{EE}}^2 + {X_{EE}}^2\right)\left(1 - {\omega_{osc}}^2 LC\right)}{\omega_{osc} L} \tag{3.3.3}$$

Also:

$$R_{EE} = \frac{1}{g_m} \tag{3.3.4}$$

$$X_{EE} = \left( \omega L_E - \frac{1}{\omega C_E} \right) \tag{3.3.5}$$

Where $R_{EE}$ is the effective negative resistance (assumes $R_e$ is large), and $L_E$ is the effective inductance of the cross-coupled pair, where $L_E = C_\pi r_b / g_m$. Equation 3.3.5 demonstrates the effect of the capacitor $C_E$ on $X_{EE}$ of the circuit, where larger value of $C_{EE}$ can be employed to create a negative $X_{EE}$. This expression can be compared to the non-degenerated case, where $X_{EE}$ is:

$$X_{EE} = \omega L_E \tag{3.3.6}$$

In Equation 3.3.6 $X_{EE}$ increases proportional to the oscillation frequency, a condition that is overcome through capacitive degeneration. Solving Equation 3.3.2 to derive the $g_m$ necessary to sustain oscillation we can write the following conditions for the non-degenerated and degenerated cases:

$$g_m > \frac{1}{R - g_m \omega L_E} \tag{3.3.7}$$

$$g_m > \frac{1}{R - g_m \left( \omega L_E - 1/\omega C_E \right)} \tag{3.3.8}$$

Where the result of the modification to $X_{EE}$ is manifested in the ability to expand the bandwidth of $g_m$. To derive new conditions for oscillation frequency of the capacitive degenerated VCO Equation 3.3.3 can be rewritten as:

$$X_{EE} = \frac{\left( {R_{EE}}^2 + {X_{EE}}^2 \right)\left( 1 - {\omega_{osc}}^2 LC \right)}{\omega_{osc} L} < 0 \tag{3.3.8}$$

This sets the following condition on the oscillation frequency:

$$\left(1-\omega_{osc}{}^{2}LC\right)<0 \tag{3.3.9}$$

$$\omega_{osc}>\frac{1}{\sqrt{LC}} \tag{3.3.10}$$

Equation 3.3.10 shows that the oscillation frequency of a capacitive degenerated resonant type VCO can be higher than the natural resonance of the tank, even if it can't be as high as predicted by equation 3.3.1. This is important for a number of reasons, the most obvious being that it enable oscillation at frequencies higher that those otherwise attainable, by allowing bandwidth extension of the cross-coupled pair. Perhaps equally important is the manner in which it relaxes the requirements of the LC tank, allowing higher inductance values to be used which achieve greater qualities. By changing the effective capacitance at the LC tank, without changing the amount of variable capacitance, we are also seeing an increase in the tuning range of the VCO. Without degeneration the tuning range (of the varactor) is $\Delta C/C*100\%$; and after degeneration it becomes $\Delta C/(C-C_e)*100\%$ (using the first order approximation).

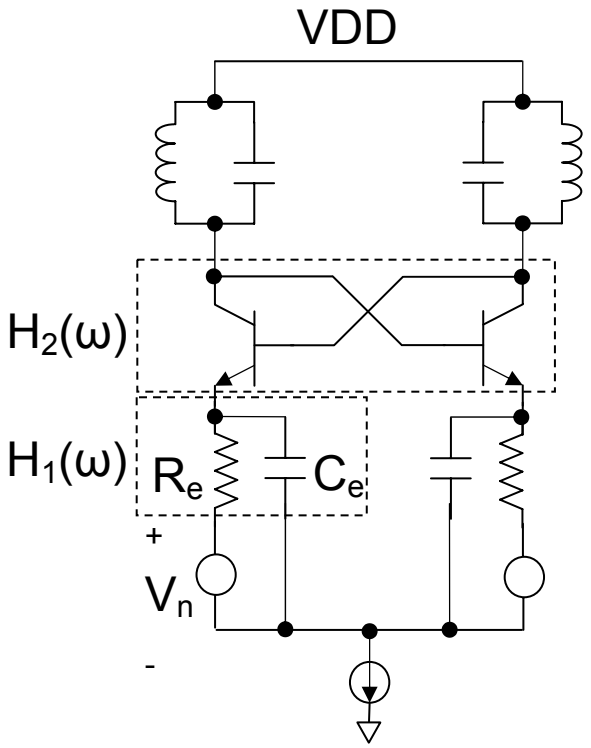



Figure 3.10: Capacitive degenerated VCO with noise and LPF effects

The ability to increase $g_m$ at high frequencies, as shown in Equation 3.3.8, has benefits beyond increased bandwidth of the cross-coupled pair. The improvements in gain of the negative resistance circuit are also manifested in increased oscillation amplitude, which improves the phase noise of the VCO as determined by Leeson's condition (Equation 3.1.4). While this improvement in noise is apparent, it would be expected that the added elements of the degeneration network would contribute to the overall noise of the system. While this is undoubtedly true, their noise impact is mitigated by the filtering effects of the degeneration network and the cross-coupled pair. In Figure 3.10 the noise sources of the degeneration network have been included, as well as the two LPF segments isolating these noise effects from the LC tank.

## 3.4 Varactor Degenerated Voltage Controlled Oscillators

Expanding on the work discussed in section 3.3 a new invention was introduced whereby the standard capacitive degeneration is implemented with a variable capacitor (varactor). The purpose of this innovation is to add additional degrees of tuning to the VCO, regarding oscillation frequency and amplitude, and achieve subsequent improvements in phase noise. While this innovation is useful for achieving greater tuning range, its achievements are primarily attributable to the fact that the condition to sustain oscillation in an oscillator is for a set tank equivalent resistance (R in equation 2.3.3). In reality the losses of a tank will vary depending upon variations in the bias conditions of the collector connected varactors, so the conditions to sustain oscillation must be set to satisfy the highest loss configuration. By introducing tuning to the degeneration network the gain of the cross-coupled pair can be dynamically adjusted to compensate changes in the biasing of the collector connected varactors, allowing for gain optimization over the entire systems bandwidth.

In Figure 3.11 a simplified model of a varactor degenerated VCO is shown. To the first order we can rewrite the expression of equation 3.3.1:

$$\omega = \frac{1}{\sqrt{L\left(C - C_e\left(V_{ct}\right)\right)}} \tag{3.4.1}$$

Where the degeneration term is now variable with some voltage $V_{ct}$. While again this solution shows the ideal case, it does demonstrate that additional tuning is now added to the VCO through degeneration capacitance, beyond the expansion in tuning range as described in section 2.3.

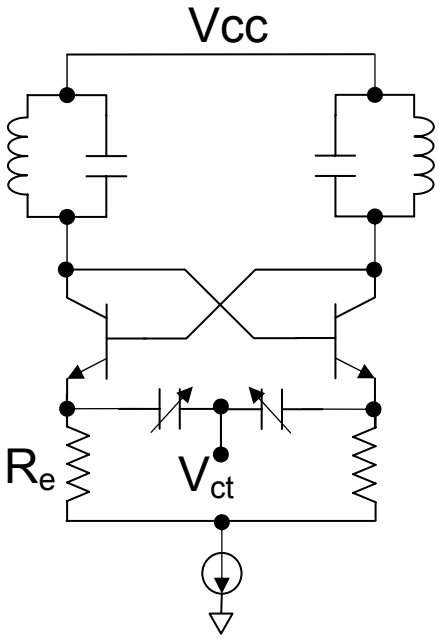



Figure 3.11: A Simplified model of a varactor degenerated VCO.

Rewriting $X_{EE}$ of the capacitive degenerated VCO to reflect the change to varactor degeneration we get:

$$X_{EE} = \left( \omega L_E - \frac{1}{\omega C_E(V_{ct})} \right) \tag{3.4.2}$$

Where $C_E(V_{ct})$ is the voltage dependent capacitance of the degeneration network. By applying this additional tuning element to the degeneration network we can further manipulate the $X_{EE}$ of the cross coupled pair, so long as we maintain the condition that $R_e >> 1/j\omega C_e$.

## 3.5 Quadrature Oscillators

A quadrature oscillator is used to create four sinusoidal (typically) outputs with 90 degree phase separation. These circuits have various applications for wireless and wireline applications, especially their ability to drive quadrature down converters or I/Q generation. Quadrature VCOs are commonly made by coupling together two (or more) VCOs, and for the purpose of the exercises described herin they will employ coupled resonant type oscillators.

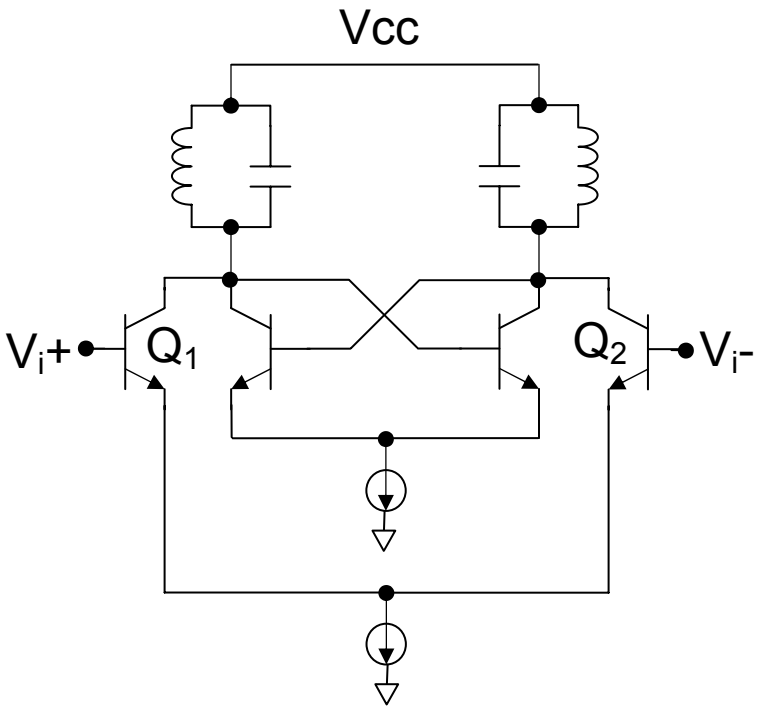



Figure 3.12: Resonant VCO with injection locking circuit

### 3.5.1 Injection Locking

The operation of these types of quadrature oscillators requires using a pair of injection locked oscillators, where the signal injected into each oscillator is provided by the companion oscillator. Consider the circuit shown in Figure 3.12, where an injection locking circuit is added to the conventional resonant type VCO. The injection

locking circuit uses devices $Q_1$ and $Q_2$ to transform the injection voltages $V_i$+ and $V_i$- into currents, which are injected into the tank of the resonant VCO. The frequency of the VCO can be manipulated by the injection signal (outside of the natural resonance of the tank) as predicted by Adler [18], where the locking range is given by:

$$f_{LOCK} = \frac{1}{2Q} \cdot \frac{V_{INJ}}{V_{OSC}} \cdot f_{OSC} \tag{3.5.1}$$

If the frequency of the injected signal is the same to the natural resonance of the VCO then the coupling can only impact the phase of the VCO, where the current through the tank (the sum of the currents of the locking circuit and the negative resistance pair) is controlled by the injected signal. It is through this behavior that a quadrature oscillator may be created through anti-phase coupling of two resonant type oscillators.

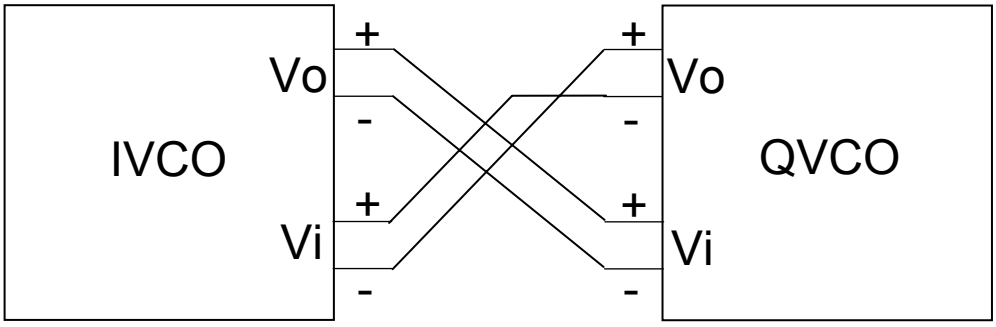



Figure 3.13: Antiphase coupled VCOs forming a quadrature oscillator

### 3.5.2 Antiphase Coupled Quadrature Oscillators

Consider a pair of resonant type VCO's coupled together as shown in Figure 3.13, where the two VCOs (IVCO and QVCO) are coupled together, where one of the

interconnects is cross-coupled. Using the concept of negative resistance this circuit can be redrawn as that shown in Figure 3.14 [12].

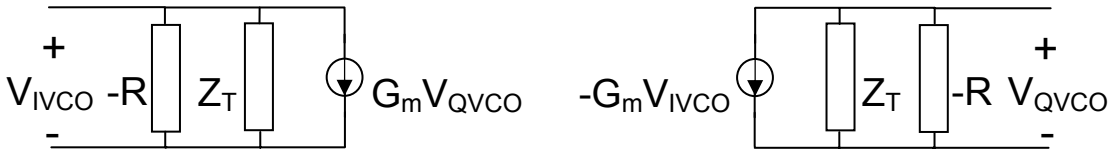



Figure 3.14: Equivalent circuit of an Antiphase coupled VCO

From this circuit the following equations can be written for $V_{IVCO}$ and $V_{QVCO}$:

$$G_m V_{QVCO} \frac{-RZ_T}{Z_T - R} = V_{IVCO} \tag{3.5.2}$$

$$-G_m V_{IVCO} \frac{-RZ_T}{Z_T - R} = V_{QVCO} \tag{3.5.3}$$

Dividing to get:

$$G_m V_{QVCO}{}^2 + G_m V_{IVCO}{}^2 = 0 \tag{3.5.4}$$

$$\therefore V_{QVCO} = \pm j V_{IVCO} \tag{3.5.5}$$

From equation 3.5.5 we can see that the two oscillators are 90 degrees out of phase (denoted by the term j), each providing differential outputs.

# Chapter 4 VCO Design Examples

## *4.1 Capacitive Degenerated Quadrature Oscillators*

A family of quadrature oscillators was designed using the capacitive degeneration technique for microwave operation [19]. The circuits were designed to investigate the high speed operations of capacitive degeneration in quadrature applications, the performance of transmission line based resonant tanks, and to compare the benefits of SiGe HBT's and CMOS for high speed buffering. Twelve oscillators were realized for operation from 14 GHz to 26 GHz with phase noise as good as – 99.18 dBc/Hz (at 1 MHz) and output powers as high as -2.5 dBm. The circuits were designed in a 47 GHz $f_t$ SiGe BICMOS technology (IBM BICMOS6HP).

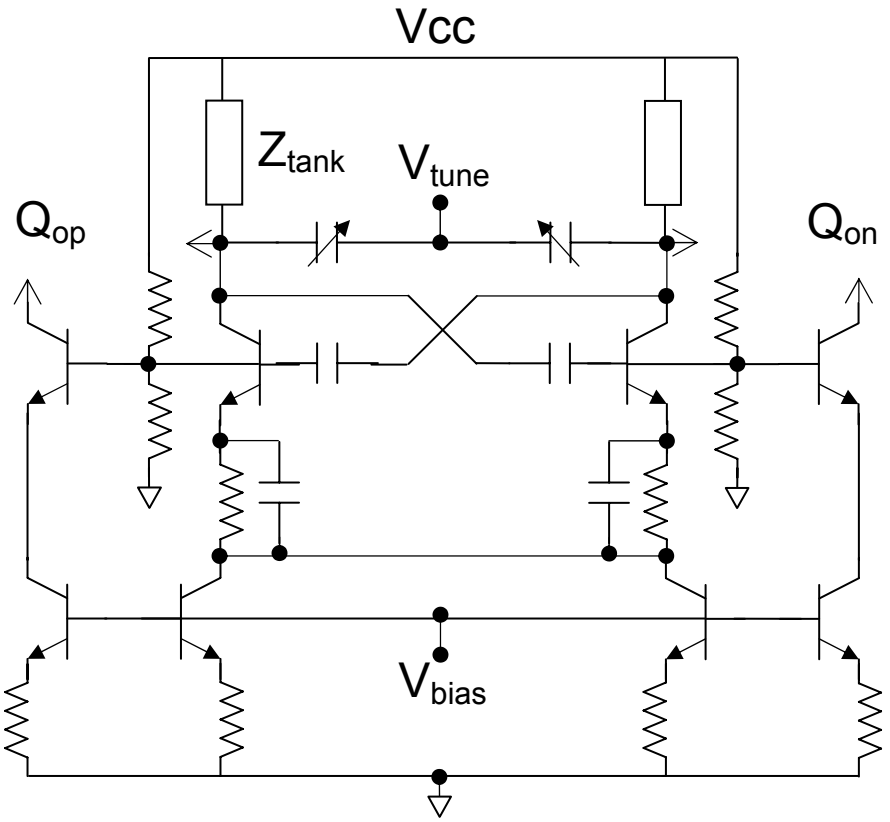



Figure 4.1: Quadrature VCO Core

### 4.1.1 VCO Core Design

Figure 4.1 shows the core of the quadrature oscillators, where the quadrature outputs $Q_{op}$ and $Q_{on}$ are connected to the interstage quadrature buffers, which are used to inject the signal from one oscillator into the tank of the companion. In this incarnation of the capacitive degenerated VCO the cross-coupled pair uses a capacitive divider to allow for a greater voltage swing across the resonant tank, with tuning provided via the pair of MOS varactors controlled via the tuning knob $V_{tune}$. Grounded coplanar transmission lines are employed for the resonator due to their improved Q at higher frequencies, their ability to be manipulated to ensure accurate common mode placement, and because they provide a local, low loss AC return path. Another important benefit of the transmission line model over the inductors is their well defined side shields, which eliminates potential coupling similar to that possible in parallel inductors. Biasing is controlled with emitter degenerated HBT current sources with a common base voltage (generated on chip). The area of the quadrature buffers is minimized to prevent excessive parasitic loading on the tank, however this limits the power injected into the tank of the companion VCO (the effects of which will be discussed in section 4.1.2).

### 4.1.2 Quadrature VCO Design

Two of the VCO cores described in section 4.1.1 are coupled together using anti-phase coupling as shown in Figure 3.13. As mentioned in section 4.1.1 the area of the quadrature buffers is minimized to prevent excessive parasitic loading on the tank, however this requires a highly symmetrical layout of the two VCO's. Following the behaviors of injection locked oscillators described in section 3.13 the small buffers (and subsequent low injection currents) will cause a small VCO locking range. As

such each oscillator must have a nearly identical oscillation frequency to its companion, to enable consistent phase locking.

### 4.1.3 50 Ω Output Buffers

Two types of 50 Ω output buffers were designed for the oscillators, one using a single stage CMOS design and the other a three stage HBT design. These designs were implemented to compare the $f_t$ and power benefits of the HBT devices to the benefits provided by the high gate impedance on the CMOS devices. The schematics of the two buffers can be seen in Figure 4.2.

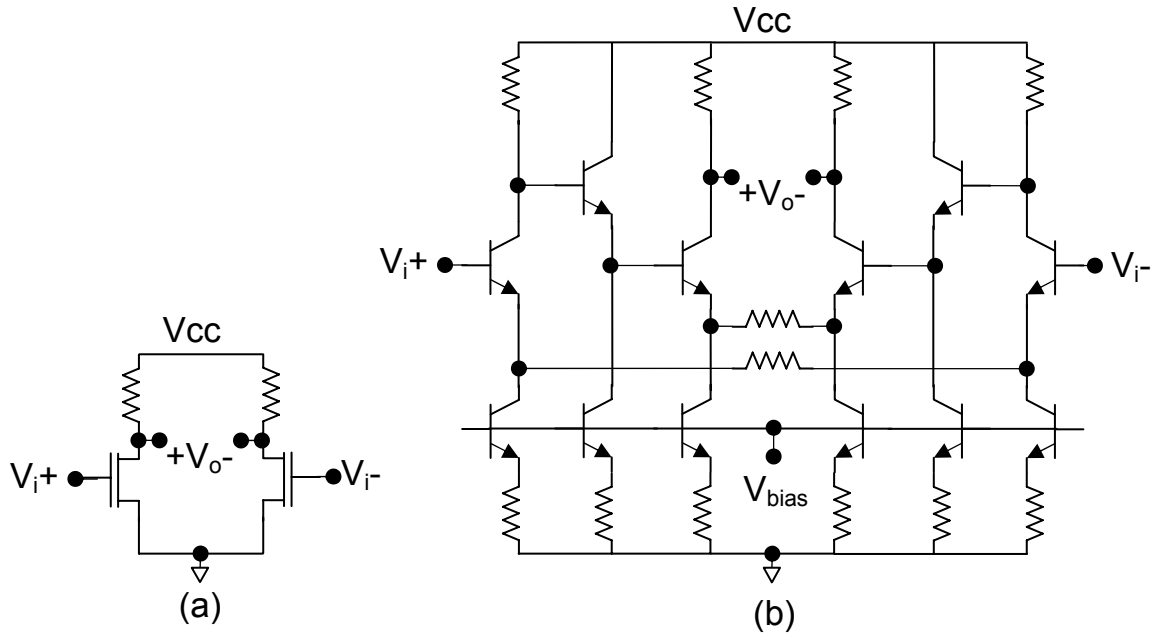



Figure 4.2 (a) One stage CMOS and (b) three stage HBT 50 Ω output buffers

In Figure 4.2 (a) the CMOS buffer is shown, where a single stage common emitter amplifier (with no tail current source) is sufficient for driving a 50 Ω load. The reason this can be achieved with a single stage is due to the high gate impedance of the

NMOS devices, which enable a large device size in a single stage buffer. The HBT buffer shown in Figure 4.2 (b) has a much lower base impedance than the NMOS gate impedance, so a large single stage buffer would load the tank of the oscillator considerably. As such the first stage must be a smaller area, requiring multiple stages to build up to a large device size suitable for driving a 50 Ω load. This considered, the HBT devices have a higher $f_t$ than the NMOS devices, and can more readily accommodate large output current and voltage swings, allowing for potentially faster operation and greater output powers. As we will later see the HBT buffers can drive larger output powers than the CMOS buffers, however even with the small input device size they load the oscillator tank more than the CMOS buffers and therefore actually cause slower operation despite their higher $f_t$.

Another benefit of the CMOS buffers is their relatively small size, enabling easy placement within the quadrature oscillator. As the circuit implements two oscillators for symmetry the most critical factor is that they be placed close together to prevent non-uniformities due to the interconnects required for anti-phase coupling. While the CMOS buffers can be designed to occupy an area less than the minimum attainable spacing between the two VCOs, the HBT buffers are much larger requiring them to be placed outside of the oscillators. This constraint requires a significant length of wiring before reaching the buffers, which further loads the tank slowing the oscillation of the VCOs.

### 4.1.4 Layout Considerations

With all high frequency design a premium is placed on a highly symmetric, low parasitic layout, however that need is further compounded with the additional wiring necessary for quadrature design. Limitations in the ability to appropriately extract and model circuit wiring make it necessary to keep extemporaneous wiring to a

minimum, and as we will see in future chapters often drive certain electrical design choices to avoid components that would require significant wiring.

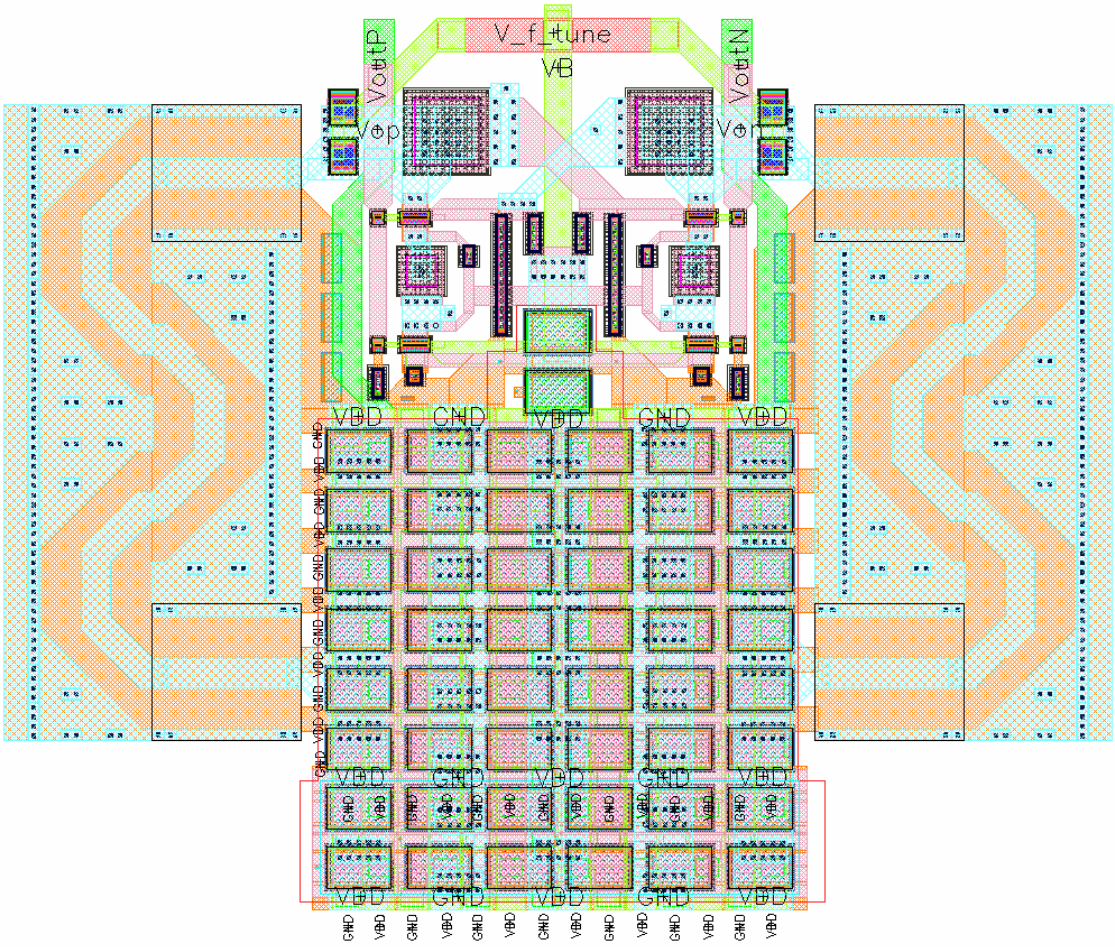



Figure 4.3: VCO layout as used to construct the quadrature VCO

In Figure 4.3 the layout of one of the VCOs that constitute the quadrature VCO can be seen. Most of the area of the VCO is consumed by the transmission lines forming the tank (as can be seen on either side of the circuit), and by decoupling for power/ground distribution (as seen at the bottom of the circuit). The active area of the VCO can be seen at the top of circuit, where the largest elements are the coupling

capacitors used to create the capacitive divider in the feedback loop. While there are electrical benefits to employing this type of divider, it can be seen from Figure 4.3 that they add considerable area to the design, as dictated by the design rules for the type of capacitors used (metal-insulator-metal/MIM). One of the biggest hurdles in miniaturization of these designs are the aforementioned technology design rules, especially as they concern deep trench isolation (DT) spacing and density. While the DT is intended to disrupt substrate currents creating greater isolation and mitigating parasitic capacitances (hence the DT lattices underneath MIM capacitors) the distance required between them often causes larger runs of wiring which actually introduce more parasitics. Beyond the introduction of these parasitics there is also the limitation of the extraction utilities to appropriately model them, which introduces a source of potential variability between simulated and measured results. It is for these reasons that it is advantageous, wherever possible, to limit wiring in high frequency designs, and in certain instances vary the electrical design to achieve this goal.

Another critical feature of the quadrature VCO is the interconnect used to cross-couple the two VCO cores. Since the derivation presented in section 3.5.2 assumes electrically transparent interconnects, it is important to make the antiphase connections short. Also, as they will inevitable have some propagation delay, it is also important to ensure that each interconnect is the same length, so that any phase shift incurred by the wiring is experienced equally by both VCO's. To further relax the effects of the interconnect a DT lattice was placed underneath the structure to mitigate parasitic capacitance to the substrate. To verify these conditions full wave modeling of the interconnect was performed using HFSS. A close-up of the interconnect can be seen in Figure 4.4.

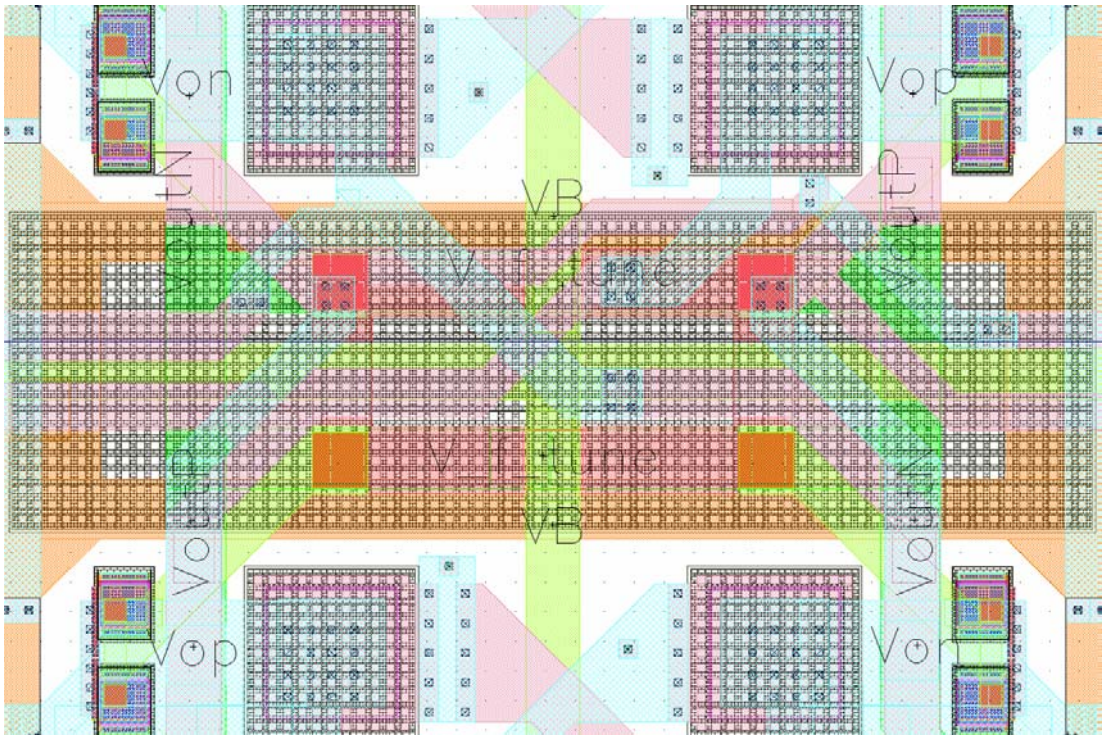
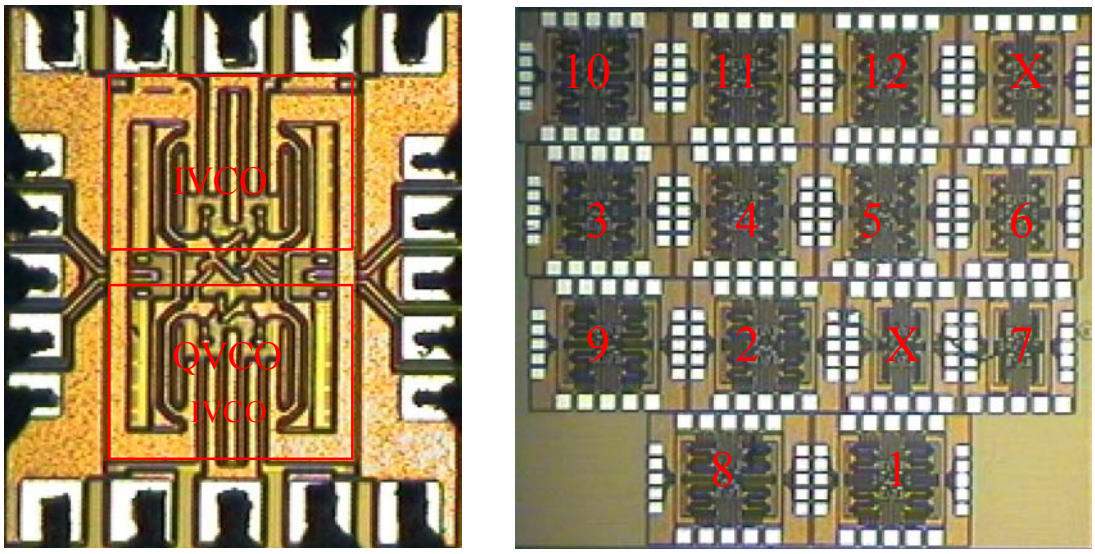



Figure 4.4: Phase matched antiphase coupling interconnect

### 4.1.5 Experimental Results

The oscillators were tested on wafer using Cascade Microtech 100 µm GSGSG and 150 µm GSGSG probes. DC biasing was provided using HP E3631A power supplies and custom batter supplies for noise critical rails. The custom supplies are necessary to eliminate low frequency noise components of typical power supplies (due to regulator switching and supply AC feedthrough) to prevent variations of DC bias points (especially VCO core VDD and varactor tuning knobs) that would degrade oscillator phase noise. Phase noise and power measurements were performed using an Agilent 8564EC 40 GHz spectrum analyzer and quadrature operation was observed using an Agilent 86100A wide bandwidth oscilloscope.




(a) (b)

Figure 4.5: (a) Die Photo of the 26 GHz VCO and (b) the entire VCO family

In Figure 4.5 photos of a close-up of one of the quadrature VCOs and the entire family of VCO's are shown. Within the family variations upon the VCO core are made by manipulating the length of the transmission line in the resonator, and for each of those variations an oscillator was prepared with both HBT and CMOS buffers.

Of the twelve oscillators presented seven employ CMOS buffers and five employ HBT buffers (two VCO's with HBT buffers would not oscillate). The VCO cores each consume 9 mA (for the two oscillators that constitute a quadrature VCO), from 2.5 V power supplies. The output buffers consume 11 mA and 31 mA of quiescent current, for the CMOS and HBT versions, respectively. The larger oscillator occupies approximately 1 $mm^2$, and the smallest 0.7 $mm^2$ (with pads). Sample output spectrums and quadrature behaviors of the oscillators can be seen in Figure 4.6.

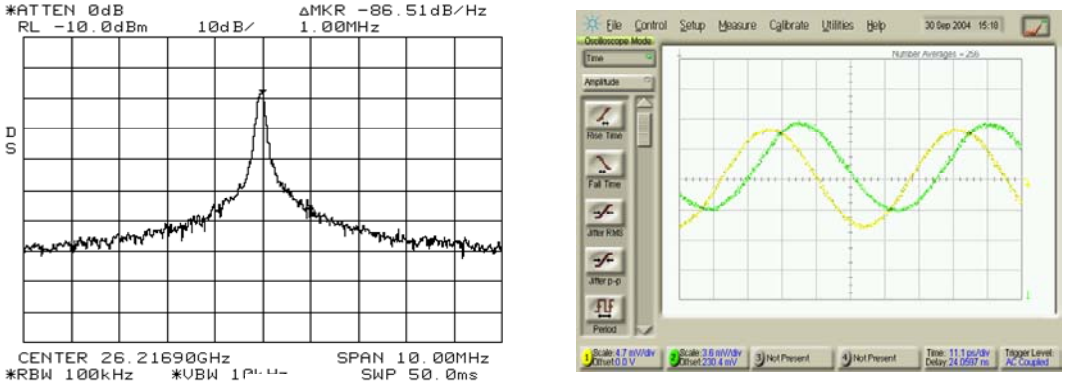



Figure 4.6: (a) Spectrum of the 26 GHz VCO (with CMOS buffers) and (b) quadrature operation (16 GHz VCO)

A summary of the results of the oscillators can be seen in Table 4.1, with comparisons of several of these oscillators (referring to their numbering from Table 4.1) to selected work shown in Table 4.2. Comparing the two different types of oscillators (CMOS vs. HBT buffered) it is evident that the higher frequency operation is obtained when using the CMOS buffers. While it was previously mentioned that this behavior was expected due to the higher gate impedance, the additional wiring required to reach the HBT buffers was actually quite substantial (as was forecast in section 4.1.3 owing to their larger size). Considering that the highest reliable impedance for a shielded transmission line (in this technology) is approximately 65 Ω, and that the buffers had to placed completely outside the VCO requiring that line length to be at least 300 μm, it is reasonable to expect that this impact is much more pronounced than the differences in gate/base impedance. Drawbacks, however, of the single stage CMOS buffer are not limited only to the lower output power. Due to the three stages employed within the HBT buffers greater low-pass filtering is achieved, attenuating harmonic components significantly more than with the CMOS buffers

(they are filtered beneath the noise floor of the system). While the CMOS buffers do still considerably attenuate these harmonics (by about 40 dB), they still have the ability to impact noise figure and linearities of components they are driving (mixers).

Table 4.1: Quadrature Oscillator Family Performance (Summarized)

| # | **Frequency Range** | **Phase Noise** | **Buffer Type** |
|---|---|---|---|
| 1 | 15.53,16.4 GHz | -92.35, -98.67 dBc/Hz | CMOS |
| 2 | 16.36,17.3 GHz | -94.68, -99.18 dBc/Hz | CMOS |
| 3 | 17.34,18.35 GHz | -94.17, -99.51 dBc/Hz | CMOS |
| 4 | 18.61,19.60 GHz | -92.85, -98.51 dBc/Hz | CMOS |
| 5 | 19.97,20.52 GHz | -95.34, -89.34 dBc/Hz | CMOS |
| 6 | 22.05,22.6 GHz | -93.51, -89.18 dBc/Hz | CMOS |
| 7 | 25.84,26.2 GHz | -86.51, -87.18 dBc/Hz | CMOS |
| 8 | 14.7,15.5 GHz | -95.84, -97.51 dBc/Hz | HBT |
| 9 | 15.39,16.30 GHz | -84.01, -94.01 dBc/Hz | HBT |
| 10 | 16.08,16.86 GHz | -83.10, -86.85 dBc/Hz | HBT |
| 11 | 17.18,18.46 GHz | -83.18, -86.18 dBc/Hz | HBT |
| 12 | 18.35,19.87 GHz | -83.51, -85.61 dBc/Hz | HBT |

Table 4.2: Comparison of SiGe Quadrature Oscillators

| Work | Max Oscillation Frequency/Ft | Output Power | Phase Noise | Tuning Range | Technology | Power Consumption |
|---|---|---|---|---|---|---|
| **[20]** | 28.9 GHz/85 GHz | -14.7 dBm | -84.2 dBc/Hz | 14% | SiGe | 129 mW (5 V) |
| **[21]** | 40 & 43 GHz/120 GHz | -11 dBm | -99,96 dBc/Hz | 12.5 %, 11.8 % | SiGe | 363 mW (3 V) |
| **[22]** | 11.8 GHz/47 GHz | NA | -103 dBc/Hz | 17% | SiGe | 105.6 mW (3.3 V) (Core) |
| **8** | 15.5 GHz/47 GHz | -2.5 dBm | -97.51 dBc/Hz | 5% | SiGe | 105.16 mW (2.5 V) |
| **11** | 18.46 GHz/47 GHz | -24.6 dBm | -86.18 dBc/Hz | 6.90% | SiGe | 47.65 mW (2.5 V) |
| **7** | 26.2 GHz/47 GHz | -25.5 dBm | -87.18 dBc/Hz | 1.50% | SiGe | 72.66 mW (2.5 V) |

## *4.2 Low Headroom Capacitive Degenerated VCOs*

Three VCOs were designed for operation from 23-25 GHz utilizing a low headroom topology [23]. The circuits employ emitter degeneration similar to the family of quadrature VCOs, however manipulations to their electrical design allows them to operate from supplies of less than one volt. Capacitive degeneration and inductive peaking were also employed for bandwidth extension in the 50 Ω output buffers, to enable operation under very low current consumptions. The circuits were designed in a 54 GHz $f_t$ SiGe BICMOS technology (IBM BICMOS7WL).

### 4.2.1 VCO Core Design

The core of the low headroom VCO employs a DC coupled capacitive degenerated core without an independent tail current. DC coupling is employed to save space and subsequently mitigate parasitics on the tank, however doing so is not

without its limitations. Foremost, since the DC bias at the base is set at VDD the cross-coupled pair cannot reliably accommodate large voltage swings across the tank the way it would be able to if it used a capacitive divider. Also, this high base voltage biases the devices in the forward active regime which incurs more parasitic capacitance at the collectors of the devices (however still less than that of a discrete capacitor). A simplified schematic of the VCO can be seen in Figure 4.7.

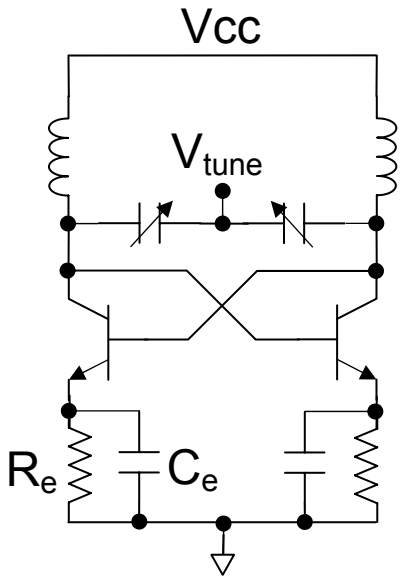



Figure 4.7: Low headroom VCO

Removing the tail current source from the VCO does introduce some other design challenges. Without an adjustable bias there is no way to adjust the current through the cross-coupled pair, which would limit the abilities to introduce features such as temperature and amplitude dependent bias manipulation, as well as making it more difficult to bias the cross coupled pair for peak $f_t$. Also, any common mode rejection that was achieved by the tail current is now removed, increasing the demands on the power structure to quell supply noise, especially at the low voltage rails

employed within this circuit. However this later shortcoming is compensated to some effect by the presence of the RC degeneration network, which acts as a low pass filter.

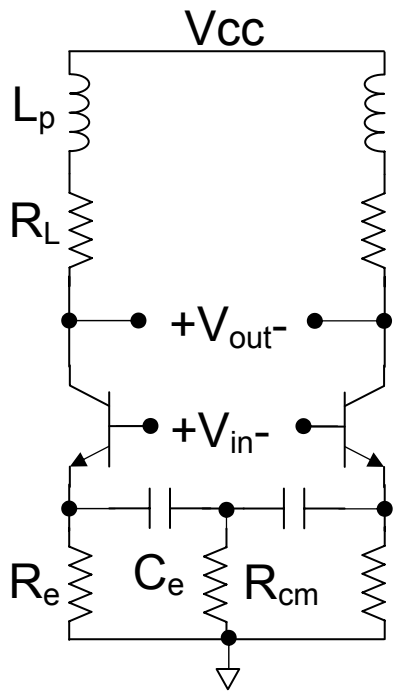



Figure 4.8: Low headroom 50 Ω buffer

### 4.2.2 50 Ω Buffer Design

To accommodate the VCO core, a broadband, low power 50 Ω buffer was designed as seen in Figure 4.8. The buffers use a pair of single-balanced common-emitter amplifiers with capacitive emitter degeneration and inductive peaking. The transistors were degenerated to increase the effective transconductance at high frequencies, with a new gain function approximated by the expression shown in equation 4.2.1.

$$G_m = \frac{g_m(2R_eC_es+1)}{2R_eC_es+1+g_mR_e} \tag{4.2.1}$$

An additional benefit is realized with this configuration by decreasing the input capacitance of the buffer stage, thereby degrading the oscillation frequency of the core (due to loading on the LC tank) less than a similarly sized buffer without degeneration. To further prevent parasitic loading on the LC tank of the oscillator core the buffers were DC coupled to the cross-coupled pair, biasing them in the forward active region (this minimizes parasitics through extra wiring and capacitors necessary for AC coupling). The inductive peaking in this circuit allows us to expand the bandwidth by resonating with the output capacitance. Since it is high impedance at the frequency of interest it also allows us to use a smaller load resistor $R_L$, which is important so that the DC bias at $V_{in}$ is near that at $V_{out}$ (circuit implemented with separate oscillator core and buffer voltage supplies to allow for independent variation of these bias points). Assuming that this buffer is driving a load impedance $Z_L$ (which, in the test environment is an AC coupled 50 Ω load), and using the result from (5), the transfer function can be written as shown in equation 4.2.2 [12].

$$\frac{V_{out}}{V_{in}} = -g_m\left(\frac{2R_eC_es+1}{2R_eC_es+1+g_mR_e}\right)\left(\frac{L_ps+R_L}{Z_LL_ps+Z_LR_L+1}\right) \tag{4.2.2}$$

### 4.2.3 Circuit Implementations and Layout Considerations

Three oscillators were designed, with the basic topologies as shown in Figure 4.9. In these designs, the LC tank as shown in Figure 4.7 is modified by the introduction of the parallel inductor $L_1$ in two of the variants (with different sized $L_1$), and parallel inductors $L_4$ & $L_6$ in the third design [22]. These inductors behave as the circuit resonator, with the series inductors $L_1$, $L_3$, and $L_5$ acting as AC chokes. Oscillators one and two differ by the size of the parallel resonator, with oscillator one

having a wider inductive line. This line exhibits a lower inductance and resistance, but at the expense of a higher parasitic capacitance. Oscillator three uses the same wide resonator as oscillator one, however also has lower inductance chokes and a second parallel resonator to attempt to raise the oscillation frequency.

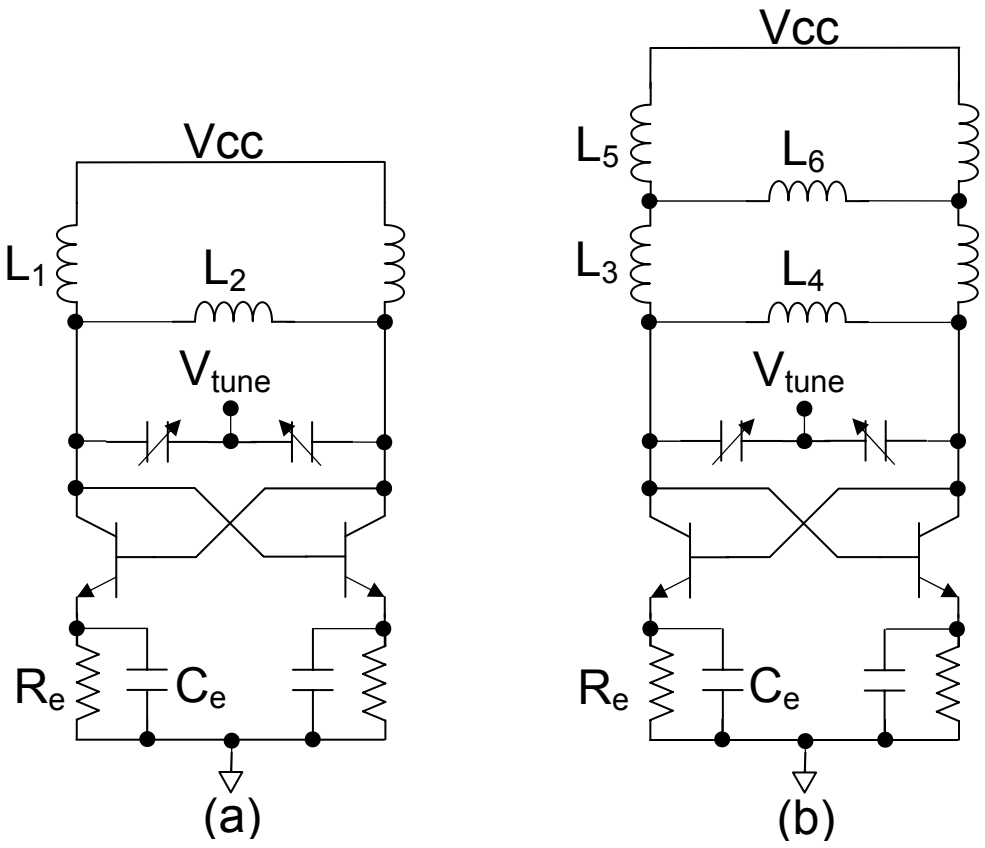



Figure 4.9: Circuit topologies for (a) VCOs one & two and (b) VCO three

Within each oscillator, a pair of MOS varactors was used for tuning, connected between the collectors of the emitter-degenerated cross-coupled pair and the tuning knob Vtune. The varactor sizes were minimized to allow for higher frequency operation, and so as not to significantly degrade the quality of the resonator. As previously mentioned, imperative in the electrical design of this oscillator was the

ability to layout the circuit so as to minimize parasitics. In Figure 4.10, the tightly packed oscillator active area (without resonator or peaking inductors) occupies a space measuring 70 µm x 80 µm.

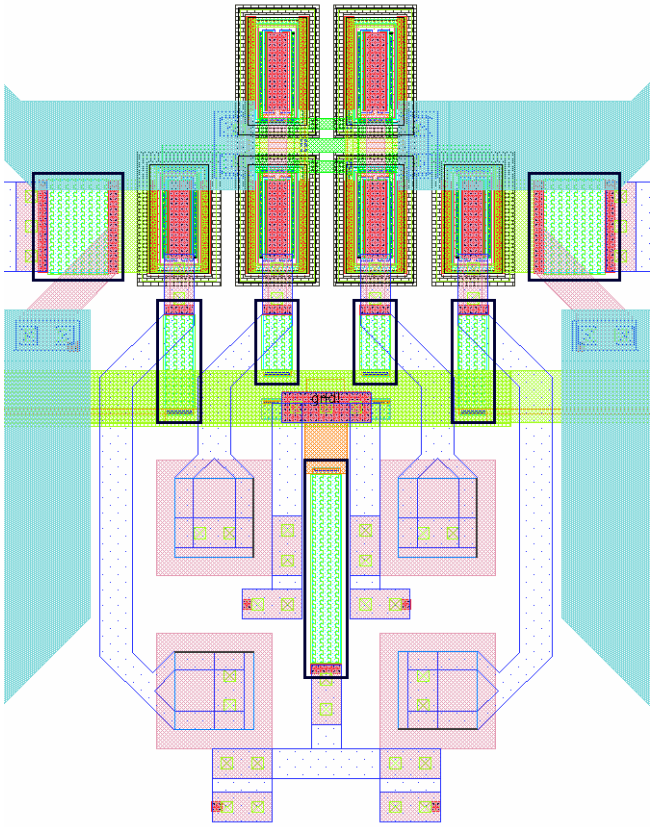
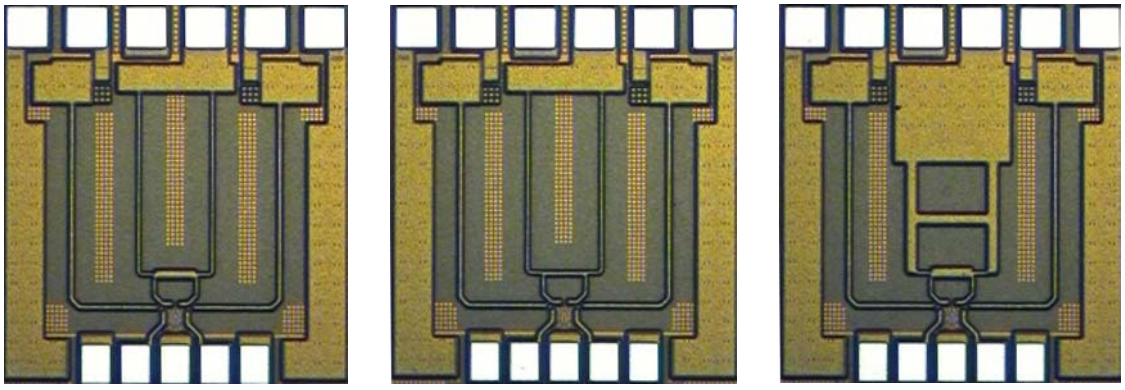



Figure 4.10: Tightly packed active area layout

Also required was a high density decoupling methodology, to quell any potential noise (as may be introduced by the oscillator or test environment) on DC nodes by creating a low impedance power network. To do this dual layer MIM (metal-insulator-metal) capacitors were employed above an interleaved metal power grid, with each ground plane thoroughly connected to the silicon substrate. Straight wire inductors were used throughout the design to realize a greater spacing between the

inductors (especially important between the core and the buffers so as not to introduce undesirable feedback), and to provide a greater quality at high frequencies (as the inductance required for the most critical, parallel inductors was quite small, straight wire inductors were more than sufficient).

In these circuits all DC contacts were provided with a six pin 150 μm pitch wedge, with two pads provided for each bias point (additional ground pads present surrounding the signal pads). All biasing throughout the circuit was provided symmetrically along the chip periphery, with the aforementioned decoupling arrays located beneath the metal ground planes that can be seen at the chip edges. Signal outputs were provided on a 100 μm GSGSG pad array, with a signal pad size of 84 μm x 100 μm to reduce parasitics. As can be seen in Figure 3.9 oscillators one and two vary in the size of their parallel resonator, with oscillator one having a wider, lower inductance inductive line. Oscillator three has the redundantly parallel resonators, with the minimum sized inductor located at the collectors of the cross-coupled pair. Die microphotographs of the three VCOs can bee seen in Figure 4.11.



(a) (b) (c)

Figure 4.11: Oscillators (a) one, (b) two, and (c) three

### 4.2.4 Experimental Results

All measurements were performed on chip, using cascade Microtech probes. 100 μm pitch GSGSG infinity probes were used for all RF connections, with biasing provided using a six pin DC wedge. All DC bias points were provided using a custom battery supply to eliminate noise effects inherent in standard supplies (especially 60 Hz noise), allowing cleaner phase noise measurements. Spectral measurements were performed using an Agilent 8564 EC 40 GHz spectrum analyzer.

All three oscillators were tested under a 1.35 V rail, with oscillator one undergoing further testing at 1.0 V and 900 mV supplies. The circuits were observed to draw between 2.5 and 9 mA of quiescent current (including buffers), for power consumptions between 2.25 and 12.15 mW. They oscillate at between 23.62 and 25.27 GHz, with output powers of between –33.5 and –8.8 dBm (with correction for cable losses). The circuits exhibit phase noise performance between –79 and –95 dBc/Hz, at 1 MHz separation. A summary of these results can be seen in Table 4.3. Representative spectral plots of the oscillators are shown in Figure 4.12.

Table 4.3: Summary of low headroom VCO results

| Oscillator | Vcc (V) | Vtune (V) | fosc (GHz) | Power (dBm) | Phase Noise (dBc/Hz) | Power Tot (mW) |
|---|---|---|---|---|---|---|
| **One** | 1.35 | 1.35 | 24.93 | -12.67 | -90.84 | 12.15 |
| **One** | 1.35 | 0 | 25.12 | -12.33 | -90.18 | 12.15 |
| **One** | 1 | 1 | 25.135 | -20.83 | -91.68 | 3 |
| **One** | 1 | 0 | 25.267 | -18 | -95.18 | 3 |
| **One** | 0.9 | 0.9 | 25.076 | -33.5 | -79.01 | 2.25 |
| **One** | 0.9 | 0 | 25.212 | -24.83 | -88.01 | 2.25 |
| **Two** | 1.35 | 1.35 | 23.62 | -12 | -86.34 | 12.15 |
| **Two** | 1.35 | 0 | 23.8 | -26.83 | -81.84 | 12.15 |
| **Three** | 1.35 | 1.35 | 24.03 | -8.83 | -90.51 | 12.15 |
| **Three** | 1.35 | 0 | 24.241 | -9.83 | -89.85 | 12.15 |

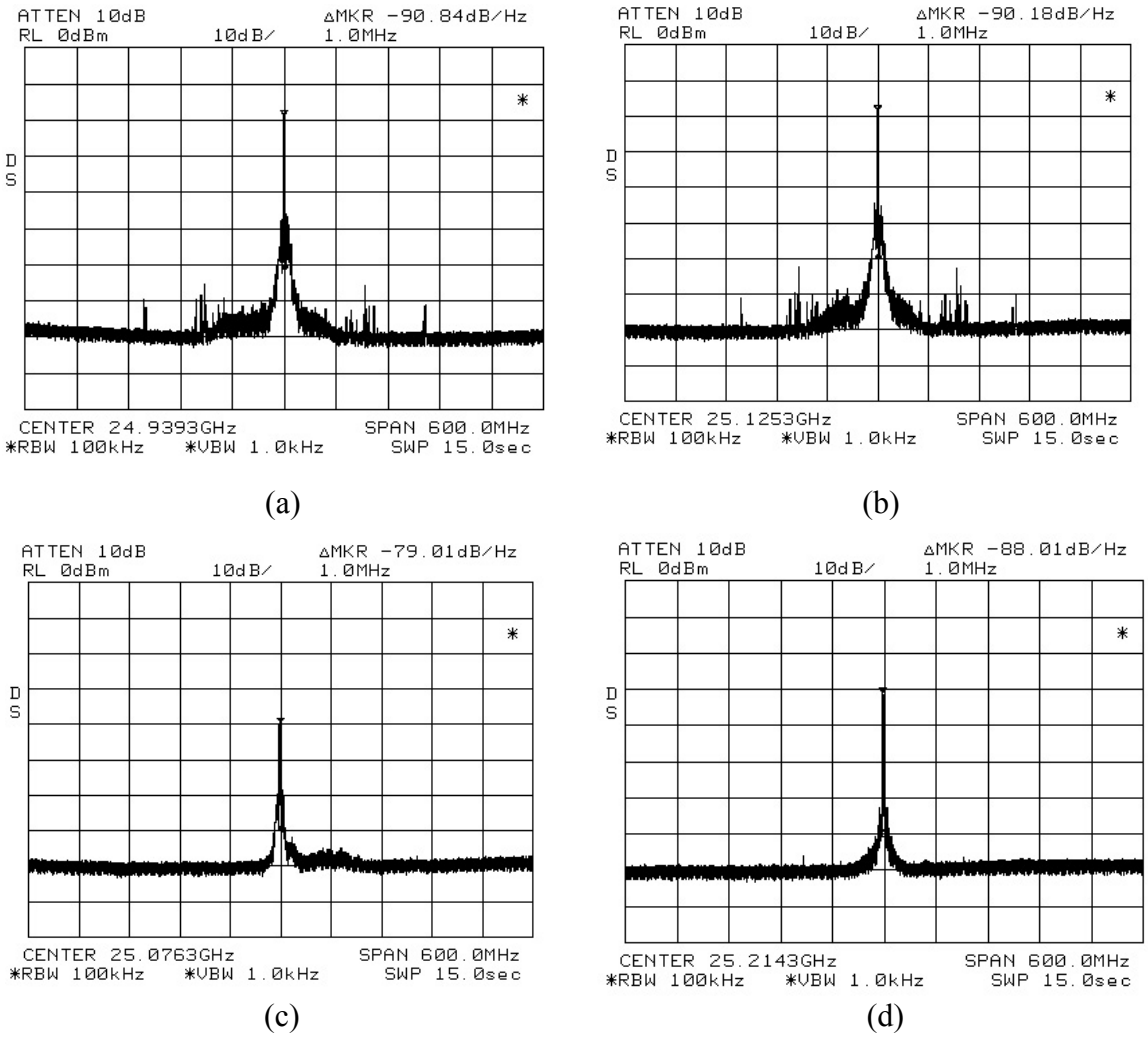



Figure 4.12: Oscillator one with (a) Vcc = 1.35 V, Vtune =1.35 V; (b) Vcc = 1.35 V, Vtune = 0 V; (c) Vcc = 900 mV, Vtune = 900 mV; (d) Vcc = 900 mV, Vtune = 0 V.

While Figure 4.1 only shows the output spectrum for oscillator one, the other two oscillators are quite similar. Comparing the oscillators as noted in Table 4.3, it can be noted that oscillator one is the most spectrally clean. As oscillator one uses a wide low inductance resonator, it also has a much lower parasitic resistance than oscillator two (but a greater parasitic capacitance). Knowing that Q = - Im(Y)/Re(Y), an increase

in the resistance (which would increase Re(Y)) decreases the tank quality and hence degrades the phase noise. Oscillator three, which has the low resistance resonator (but modified AC chokes), has similar phase noise performance, but here by diminishing the inductance of the AC chokes we are again diminishing the tank quality. Notwithstanding these differences, all three oscillators exhibit good phase noise performance at nearly half the available $f_t$, while being capable of performing under very low supply voltages with minimal power consumption. A comparison to other works can be seen in Table 4.4.

Table 4.4: Comparison to published works

| Oscillator | Vcc (V) | fosc/ft (GHz) | Range (MHz) | Power (mW) | CNR (dBc/Hz) | Technology |
|---|---|---|---|---|---|---|
| **One** | 1.35 | 25.025/54 (46.3%) | 190 | 12.15 | -90.51 | SiGe |
| **One** | 0.9 | 25.144/54 (46.6%) | 136 | 2.25 | -83.51 | SiGe |
| **[24]** | 1.9 | 24.89/47 (53%) | 1300 | 27 | -81 | SiGe |
| **[20]** | 5 | 26.85/85 (31.6%) | 4100 | 129 | -84.2 | SiGe |
| **[25]** | 3.5 | 21.65/80 (27%) | 2300 | 119 | -104 | SiGe |
| **[26]** | 1.5 | 38.6/NA (NA%) | 3000 | 17.25 | -109.73 | SOI CMOS |

## *4.3 mmWave Varactor Degenerated VCOs at 50 GHz*

The first foray into true mmWave VCO design was done using a 120 GHz $f_t$ SiGe BiCMOS technology (SiGe BiCMOS7HP), with a varactor degenerated core. Here a VCO was designed for operation from 47-50 GHz, also demonstrating a new method for implementing the resonant tank using circular transmission lines.

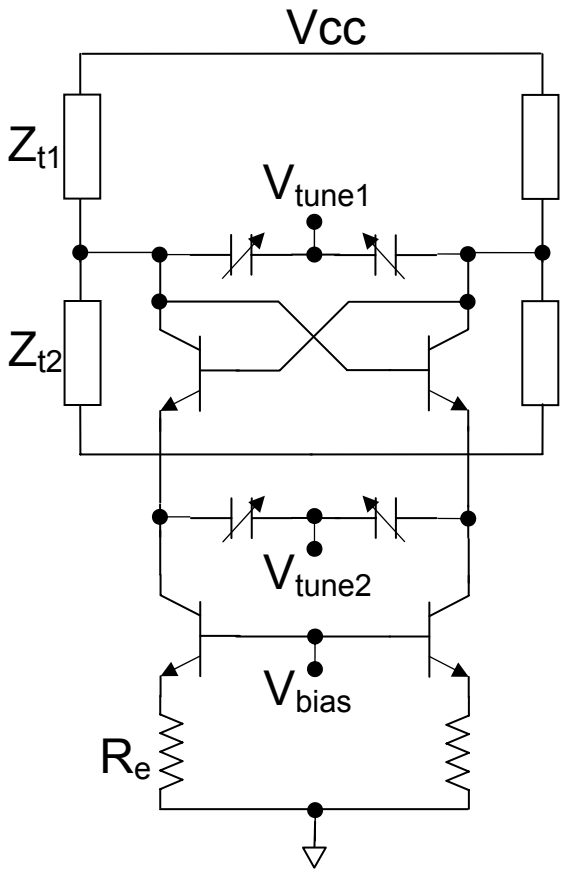



Figure 4.13: 50 GHz varactor degenerated core

### 4.3.1 VCO Core Design

In Figure 4.13 the core of the VCO can be seen, where the emitter degeneration is achieved using a pair of MOS type varactors. In place of a resistive load the cross-coupled pair uses independent degenerated current sources to create a high impedance path to ground. Doing so enables external manipulation of the bias current of the VCO, without substantially increasing the headroom required. Including these tail currents allows us to use a cross-coupled pair with a small area (so as not to excessively load the tank) with an aggressive bias to still achieve a large voltage swing across the resonant tank. The circuit uses DC coupling to mitigate the parasitic effects

of the large area MIM capacitors needed for a capacitive divider, and employs a two element transmission line based tank to achieve a higher Q and achieve more uniform current distributions. This tank used coupled grounded coplanar transmission lines placed at a close separation to mitigate wiring parasitics, and rests directly above the active portions of the VCO core forcing all wiring to be orthogonal to the substrate. This will be discussed more thoroughly in section 4.3.3.

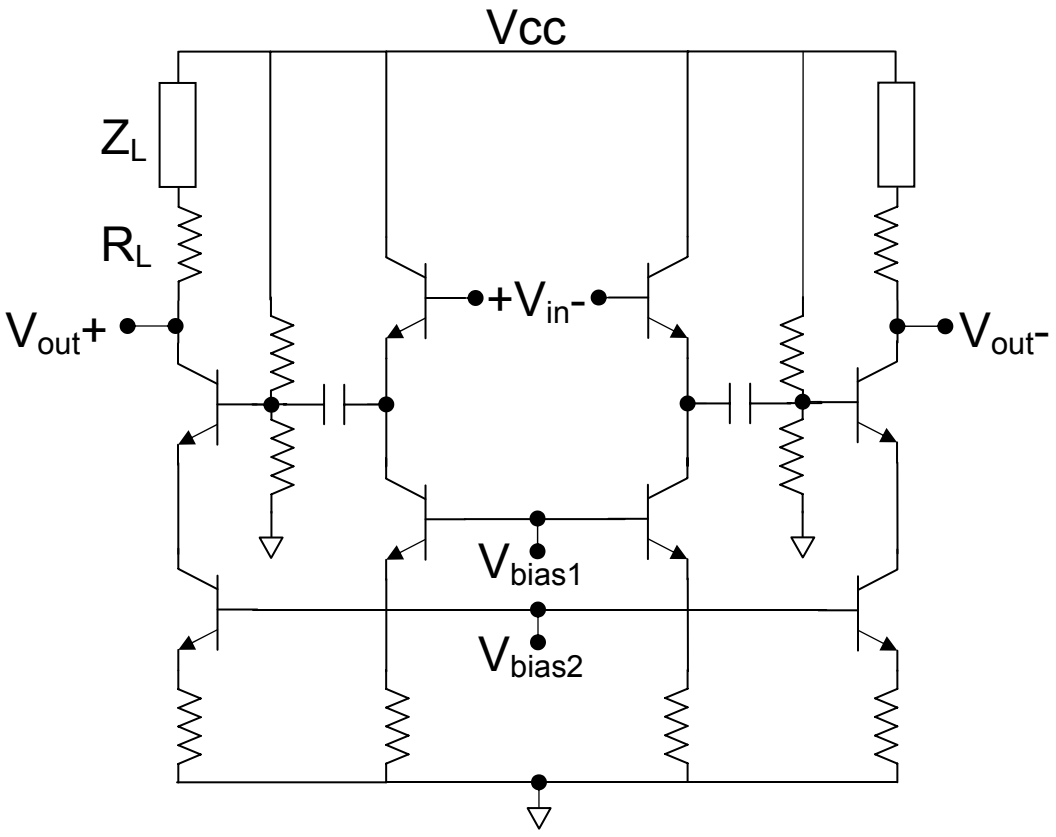



Figure 4.14: 50 GHz 50 Ω buffer

### 4.3.2 50 Ω Buffer Design

The VCO employs a two stage 50 Ω buffer design as shown in figure 4.14. Here a pair of emitter followers are DC coupled directly to the LC tank, which prevents excessive loading on the VCO core. A pair of inductively peaked common emitter pairs with independent tail currents (functioning also as degeneration) are AC coupled to the follower outputs, with inductive peaking achieved using grounded coplanar transmission lines. Employing two stages enables using a large device size to drive the 50 Ω load, while isolating the tank from the low base impedance of the device.

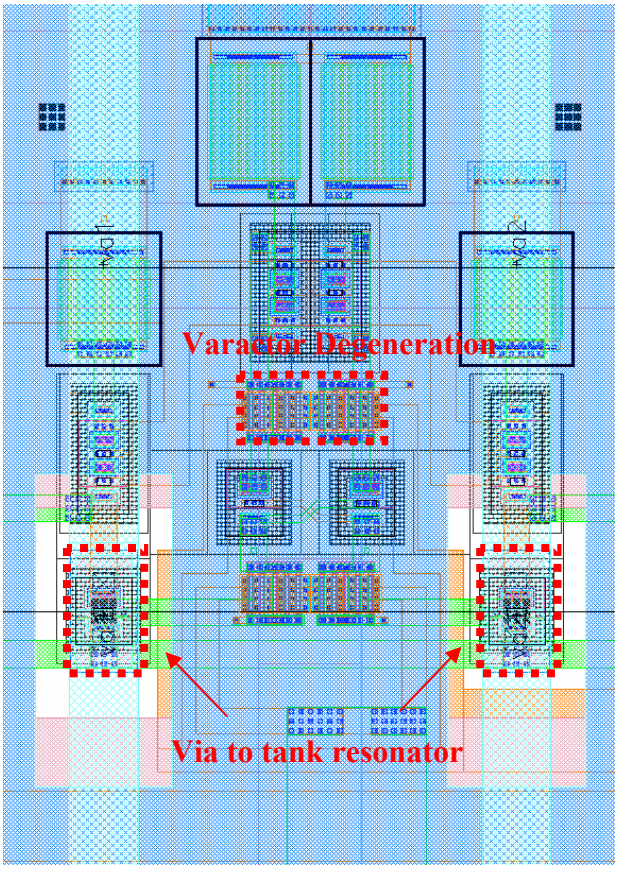



Figure 4.15: 50 GHz VCO active area

### 4.3.3 Layout Considerations and Resonant Tank Placement

One of the added benefits of varactor degeneration, beyond fixed capacitance degeneration, is it employs a FEOL (front end of the line) capacitor as opposed to the large aspect ratio MIM capacitors. This benefit is realized in a drastic reduction of VCO core size, and a subsequent mitigation of unmodeled parasitics (note that the FEOL varactors are lower quality than MIM capacitors, but since they require less wiring they introduce less potential variability into the design). This use of varactors, combined with DC coupling of the cross-coupled pair, allows us to achieve a small VCO active area, as shown in Figure 4.15. In Figure 3.15 the VCO core and first stage of VCO buffering are shown to occupy and area of 30 μm x 40 μm. Also shown in Figure 4.15 are the vias used to connect to the transmission line based resonator, which are outlined in red. By having such a compact active area it is possible to place the resonator directly above the VCO using only these two vias as interconnects, with the transmission lines backplane able to shield the active area from the resonator, and thoroughly deliver ground throughout the circuit.

Another feature of the coupled wire transmission line based tank is that it enables precise location of the common mode point of the two branches of the oscillator, which helps to alleviate the demands on the decoupling to provide an AC current return path. As discussed in chapter 3, this is crucial in high frequency design because even in the presence of very dense coupling there is still limited ability for them to provide reasonable returns due to the low capacitance densities possible on chip. By using the differential half to perfectly quell the common mode, the decoupling throughout the structure is only needed to quite any evanescent noise sources. A close up of the technique used to achieve this accurate common mode node, whereby the two transmission lines meet and the bias is provided orthogonally

from bellow, can be seen in Figure 4.16. A die microphotograph of the VCO can be seen in Figure 4.17.

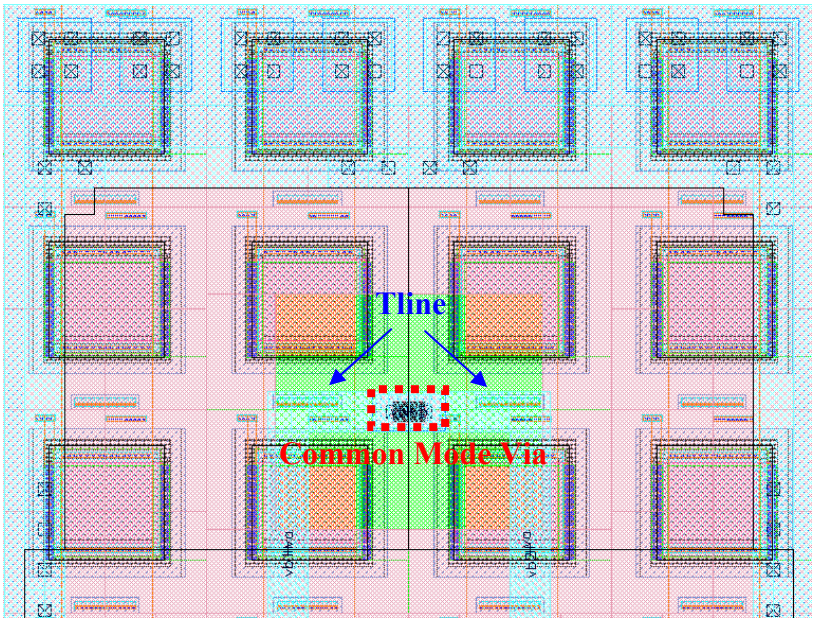



Figure 4.16: Common mode placement technique

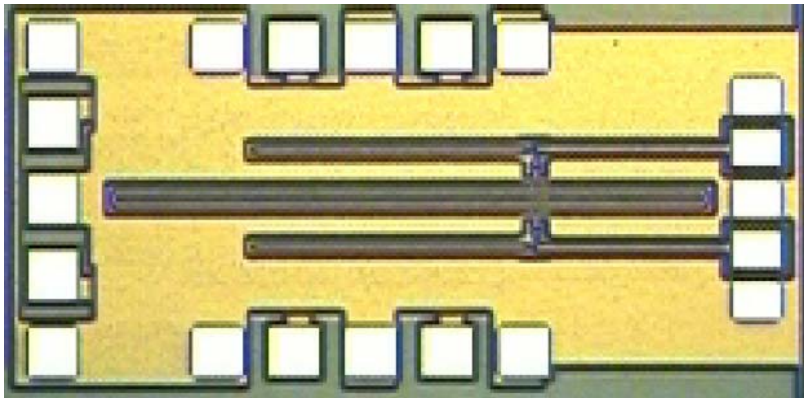


Figure 4.17: 50 GHz VCO Die Photo

### 4.3.4 Experimental Results

The oscillator described above was tested on wafer using Cascade Microtech 100 μm infinity probes. Similar to previous VCO testing low noise supplies (batteries) were used on critical rails to mitigate their effects of the oscillators phase noise. One increasing challenge with high frequency measurements is the ability to accurately lock and maintain the peak of the VCO spectrum, which can lead to degradation of noise and power measurements (which is compensated in the measurement techniques of later designs). This is manifested foremost when using a small sampling window to get an accurate measurement (at a small spacing); however these tight sampling settings are necessary in order to achieve a low noise floor in the measurement. A sample spectrum of the oscillator (tuned to 47 GHz) can be seen in Figure 4.18 (note that the upper limit of the spectrum analyzer used to test this circuit was 50 GHz, able to demonstrate functionality up to the frequency but unable to generate useful spectral displays). The circuit consumes 19 mW of power off a 2.25 V power supply while outputting -14 dBm of power.

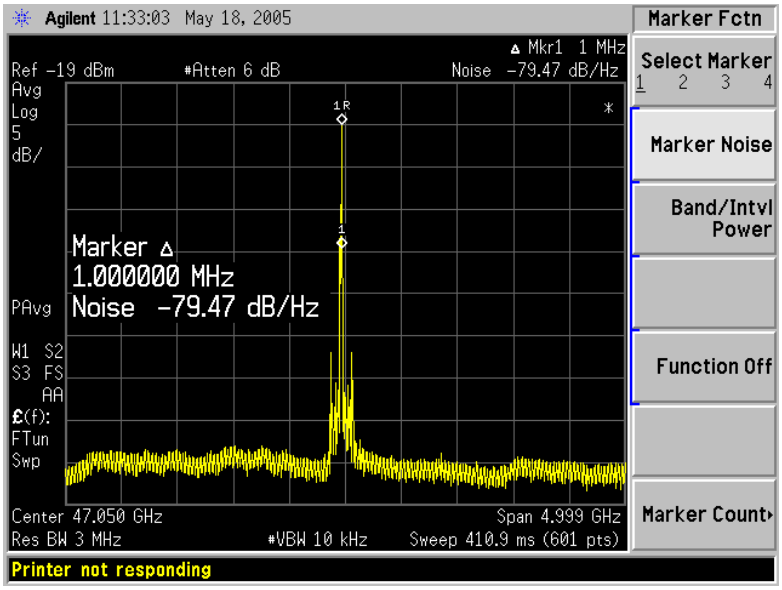



Figure 4.18: 47 GHz output spectrum

## 4.4 A High Power Varactor Degenerated VCO at 60 GHz

A high power VCO was designed for use as a radio transmitter in the 59-64 GHz ISM band [27]. The circuit is designed to be used to either drive directly into a PA with some modulation applied to the VCO, or as a high powered local oscillator for use with a passive (Schottky type) mixer, in either a transmitter of receiver. This circuit is designed to achieve very high output powers while still achieving very low phase noise, using a 206 GHz $f_t$ SiGe BiCMOS technology (BiCMOS8HP).

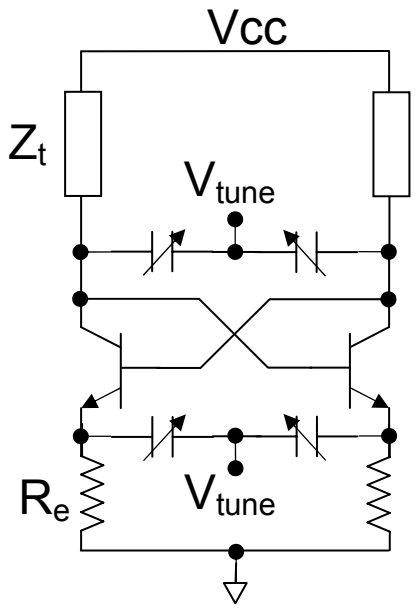



Figure 4.19: Varactor degenerated VCO core

### 4.4.1 VCO Core Design

The core of the VCO can be seen in Figure 4.19, where it employs a DC coupled varactor degenerated cross-coupled pair without applied tail current source. The varactor degeneration shares a common tuning knob with the collector connected tuning varactors, due to limited pin availability. The resonant tank is created using a pair of coupled 65 Ω transmission lines (single mode impedance), and a pair of MOS

varactors. Coupled wires are used due to their compact geometry, enabling them to be connected to the cross-coupled pair with minimum unmodeled wiring. To further mitigate parasitics the transmission line resonator is placed directly above the cross-coupled pair so that all wiring is done orthogonally to the substrate, however here the resonator only uses a single pair of transmission lines to enable placement of degeneration transmission lines in the output buffers.

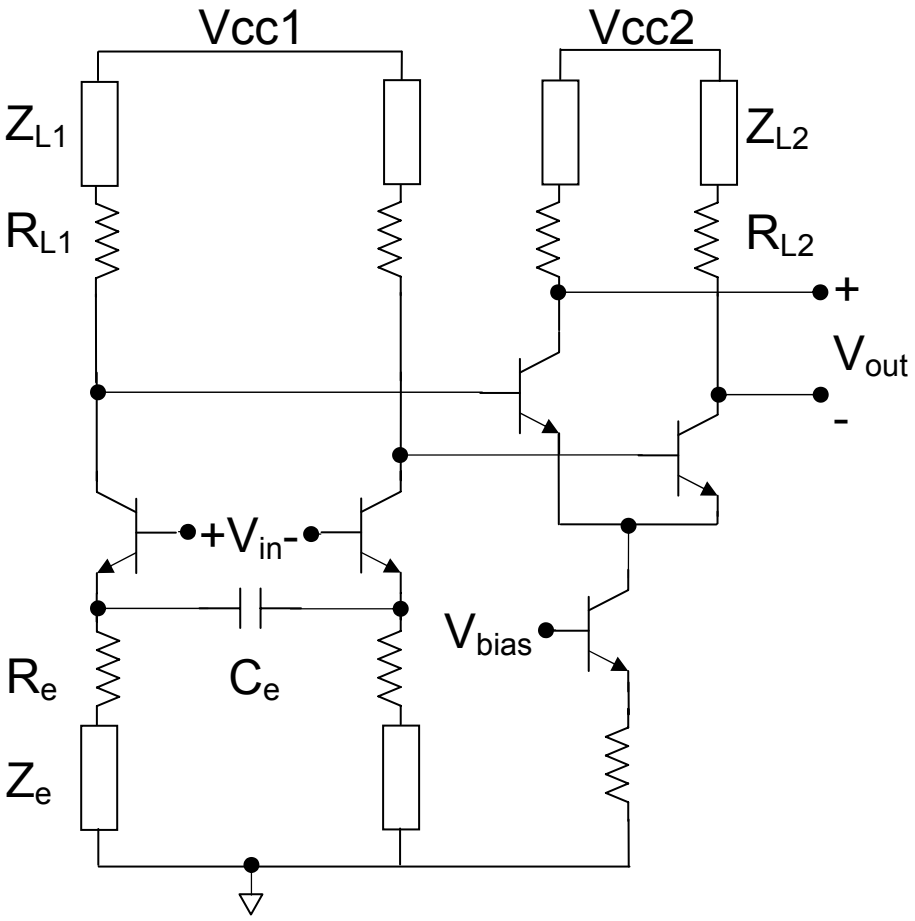



Figure 4.20: Two stage 50 Ω buffer

### 4.4.2 50 Ω Buffer Design

In this design a high powered buffer was required to be able to drive a power amplifier for applications of a directly modulated VCO transmitter. To that end several new design challenges were present, beyond the high saturation power of the output stage. Since the final stage required a large area to drive 8 dBm of power, multiple buffering stages were required to inhibit the output stage from excessively loading the VCO tank. As a large amount of gain was required employing a first stage follower was not the preferred method, and a common emitter stage was instead employed due to its much higher gain. Also crucial in the physical design of this circuit is the power distribution and decoupling methodology, as large currents are required to produce the high output power. To that end the entire chip is consumed by a stacked decoupling cell which has redundant planes to distribute power and ground and staked capacitors to achieve a high capacitance density (MIMs above MOScaps). A schematic of the two stage buffer can be seen in Figure 4.20.

In the buffer two separate supplies are provided, where Vcc2 is a 4V supply (common to the companion power amplifier), to enable easy bias manipulation. Separate supplies (Vcc1 is 2V and Vcc of the VCO core is 1V) enables DC coupling (without level shifting) between the different stages to inhibit parasitics that may be created by MIM capacitors used for AC coupling. Similar to the oscillator described in section 4.2, the first stage of buffering is a DC coupled common emitter stage, employing emitter degeneration to increase the base impedance of the HBT. In addition to using capacitive degeneration and inductive element is added in series with the degeneration resistance (by way of a transmission lines), which increased the isolation from ground at higher frequencies. In both stages inductive peaking is employed to move the output pole of the HBT higher in frequency, and reduced resistive loads are employed to further expand the bandwidth.

### 4.4.3 Power Amplifier

The highest output power variant of this VCO uses a cascoded class AB push-pull power amplifier to generate as much as 17 dBm of output power. A simplified schematic of the PA can be seen in Figure 4.21.

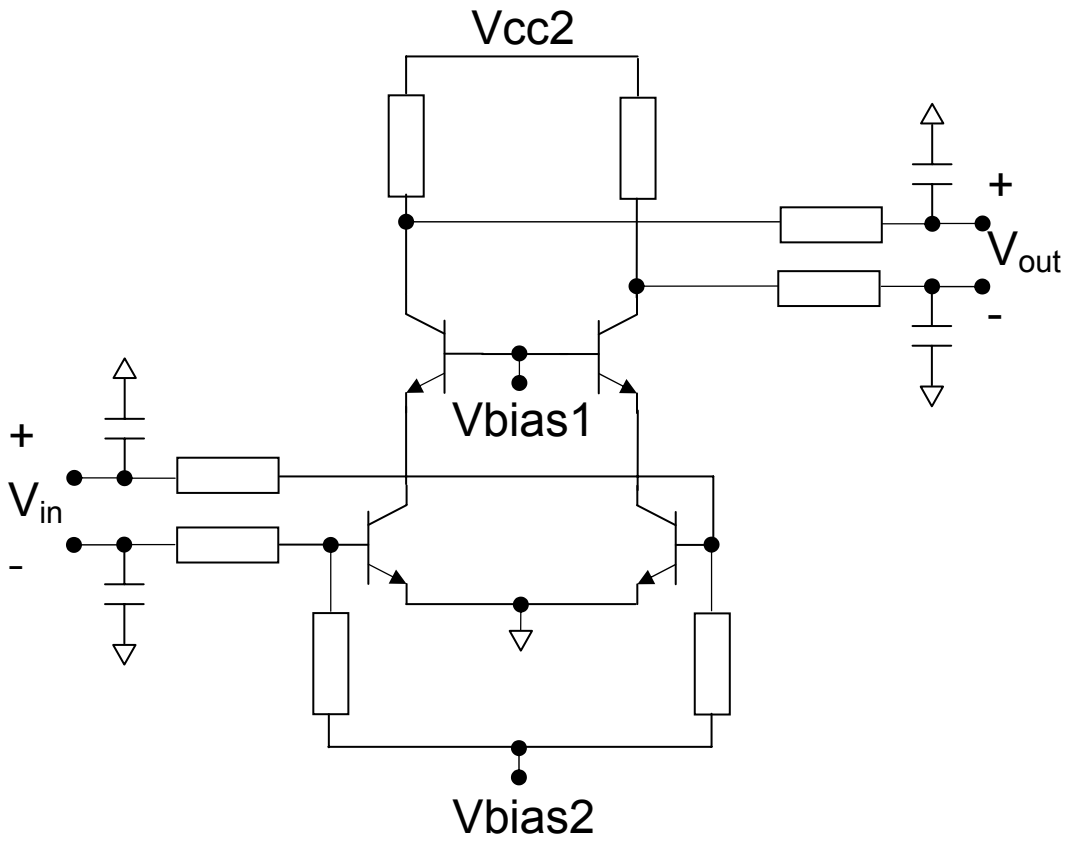



Figure 4.21: Simplified class AB PA

### 4.4.4 Experimental Results

The VCO and VCO/PA combo were both measured on chip using 150 μm GGB microwave probes and decoupled power supply wedges, with three different

voltage rails provided with Vcc = 1V, Vcc1 = 2V, Vcc2 = 4V. Harmonic downconversion was necessary for phase noise measurements, with a weak tone injected into the differential port to stabilize the measurement. Differential measurements were also performed employing a waveguide (WR-15) Balun and coupler for signal injection, yielding identical noise measurements to the single ended case. Power measurements for both the VCO and VCO/PA combo were obtained using a separate power meter. The output spectrum of the VCO can be seen in Figure 4.22.

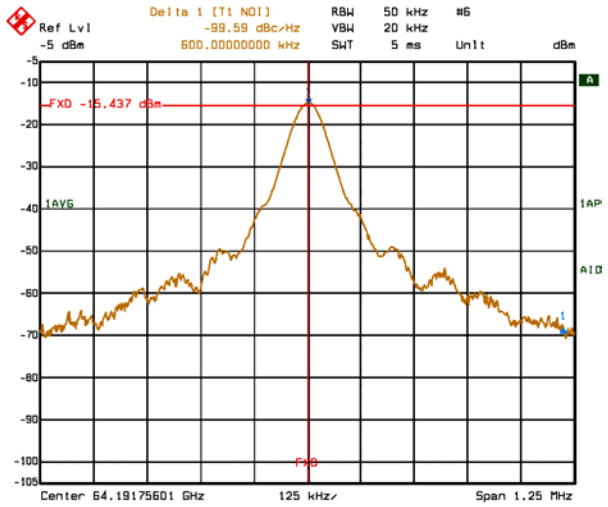



Figure 4.22: VCO output spectrum showing phase noise of -100 dBc/Hz (at 600 kHz separation)

In Figure 4.22 the phase noise of the VCO is shown to be as good as -100 dBc/Hz at 600 KHz separation. Due to noise floor limitations of the test equipment involved noise measurements beyond 600 kHz separation show negligible difference (this is primarily due to the noise limitations of the harmonic downconverters). Using an external power meter, which is coupled to the output through a WR-15 type branchline coupler, the output power of the VCO can be measured simultaneously to the phase noise. A figure of merit for the VCO can be extracted from [28]:

$$FOM = CNR + 20\log\left(\frac{f_{off}}{f_c}\right) + 10\log(P_D) \quad (3.4.1)$$

From equation 3.4.1 the FOM of the circuits are -172 and -180, with and without the PA. This FOM is one of the highest recorded for a Silicon VCO, exceeding previous high power mmWave silicon VCOs presented in [29]. A summary of the results of the VCO can be seen in Table 4.5, a die photo of the circuit can be seen in Figure 4.23.

Table 4.5: Summary of 60 GHz VCO/PA combo performance

| | |
|---|---|
| Tuning Range (GHz) | 62 to 64 |
| Output Power (dBm) | 17 (5 without PA) |
| Phase Noise 600 KHz (dBc/Hz) | -100 |
| Vdd (V) | 1,2,4 |
| Ptot | 130mW to 630 mW |
| FOM (dB) (With PA/Without) | -172/-180 |
| PFN (dB) (With PA/Without) | -1.4/6.6 |
| PFTN (dB) (With PA/Without) | -31.4/-23.4 |

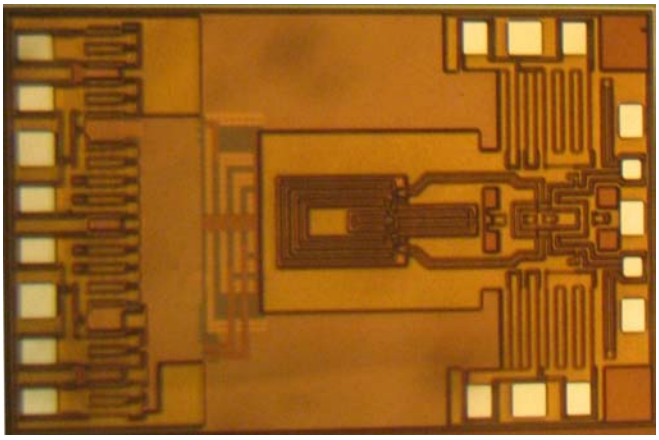


Figure 4.23: 60 GHz High Power VCO Die Photo

## 4.5 Conclusions

In this chapter a family of voltage controlled oscillators were developed to push the abilities of silicon technologies into the mmWave regime. In so doing certain techniques were shown to be imperative to the design cycle, techniques that act to quell the effects of circuit parasitics. Among these techniques are DC coupling in the feedback path of the oscillator, which eliminates the parasitic capacitance of a MIM capacitor with the substrate, and coupled transmission line resonators which limits the amount of wiring necessary to connect the VCO core to its tank.

Employing these techniques oscillators were developed to run up to 60 GHz and beyond, without unacceptable degradation of output power or phase noise. Early results of continued work beyond that described here shows that these techniques will continue to enable the creation of mmWave silicon VCOs up to and beyond 100 GHz.

# Chapter 5 LNA Design and Innovation

## *5.1 LNA Fundamentals*

Low noise amplifiers (LNAs) are employed in the receivers of many wireless systems and are often vital to their performance. They must be able to operate while simultaneously contributing very little noise to the input signal, amplifying the signal significantly enough to mitigate the noise effects of later stages, and accommodate a large range of input powers, typically while consuming very low power. An example of a wireless transceiver demonstrating the placement and application of the LNA can be seen in Figure 5.1.

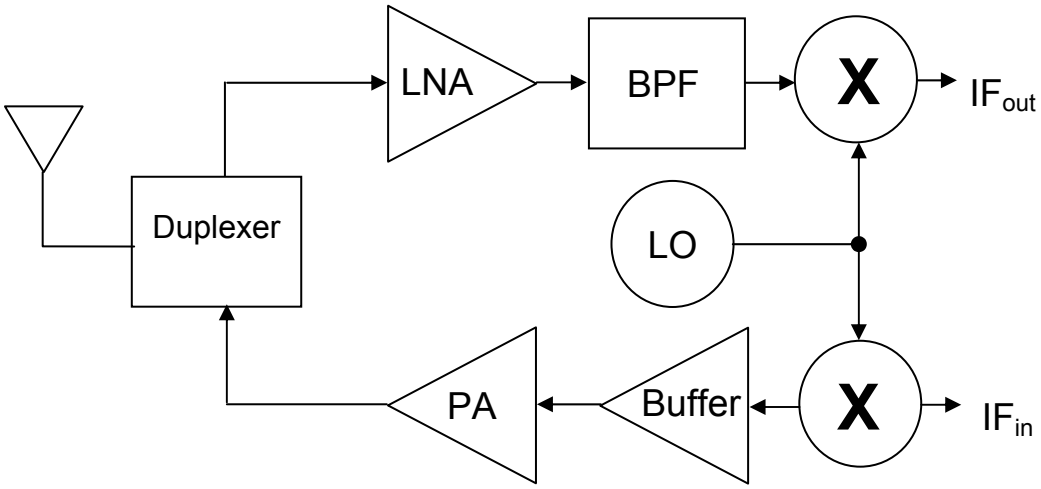



Figure 5.1: A simplified transceiver front end block diagram

In Figure 5.1 the LNA is the first active circuit in the receiver path of the transceiver. Assuming that the noise contributions of the antenna and duplexer are small (vital for a functional transceiver), the LNA is the most noise sensitive circuit in the system. Consider the following relationship for determining input referred noise of a receiver containing m cascaded stages [30]:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \frac{NF_3 - 1}{A_{p1}A_{p2}} + .... + \frac{NF_m - 1}{A_{p1}....A_{p(m-1)}} \quad (5.1.1)$$

Where $NF_m$ is the noise figure and $A_{pm}$ is the available gain of stage m. From this relationship it can be seen that beyond achieving low noise the LNA can lower the overall noise figure of the system by achieving high gain. In most receivers the contributions of the later stages are but a fraction of that of the LNA on the total system noise figure, however this may not be the case in instances of an exceptionally low LNA noise figure or gain.

### 5.1.1 Noise Sources in an LNA

Recalling the noise model for HBT's and CMOS devices as described in section 3.1 we have the model redrawn in Figure 5.2.

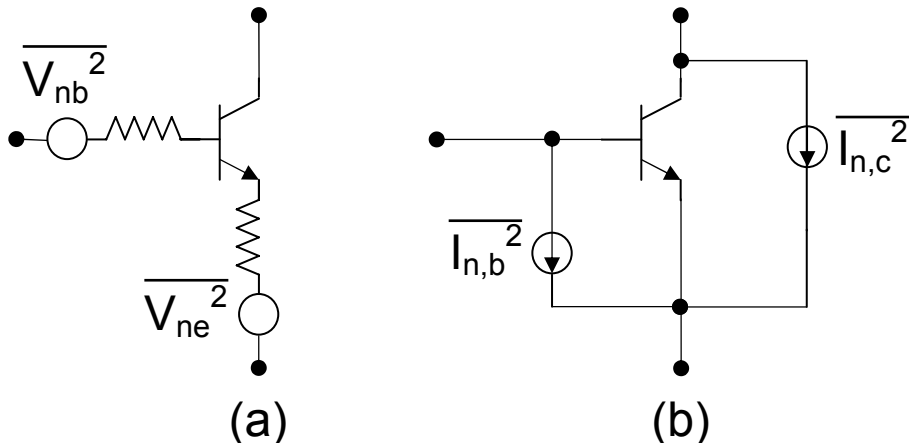



Figure 5.2: Transistor (a) Thermal noise and (b) shot noise

$$\overline{V_n^2} = 4kTR\Delta f \ , \ \overline{I_n^2} = 4kT\left(\frac{2}{3}g_m\right) \quad (5.1.2)$$

$$\overline{I_n^2} = 2qI \quad (5.1.3)$$

$$\overline{V_n^2} = \frac{K}{WLC_{ox}} \frac{1}{f} \tag{5.1.4}$$

Where the thermal noise current source $I_n$ in equation 5.1.2 is the equivalent thermal noise current parallel to the CMOS device (source to drain connected).

While the noise sources described above can be controlled (to some extent) by manipulation of the devices used, this is often at the expense of optimization of other parameters of the circuit in which they are employed. From equation 5.1.2 the input referred noise (per unit bandwidth) is:

$$\overline{V_n^2} = 4kTR \tag{5.1.5}$$

Where the equivalent input resistance, R, can be written as [9]:

$$R = \left( r_b + \frac{1}{2g_m} \right) = \left( r_b + \frac{V_T}{2I_C} \right) \tag{5.1.6}$$

Showing the input referred thermal noise to be:

$$\overline{V_n^2} = 4kT\left( r_b + \frac{V_T}{2I_c} \right) \tag{5.1.7}$$

Suggesting that a larger $I_c$ ($g_m$) of the device will lead to a lower input referred noise. Increasing this drive current, however, will lead to an increase in the shot noise for each device, which is proportional to the drive current of the transistor, as shown in equation 5.1.3. Beyond this hurdle, frequency dependent limitations are introduced with increased $g_m$ of the transistor, as will be discussed in section 5.1.2. CMOS also

has the additional noise element of flicker noise, which arises from trapped charge at the oxide-silicon interface. This noise effect, demonstrated in equation 5.1.4, also shows a dependency on device gain through it's variation with device area (Dependence of W, L, and $C_{ox}$). It is out of these concerns, and the requirements of matching of the circuit (50 Ω for the examples described herin), that noise figure is one of the most challenging tradeoffs in wireless design.

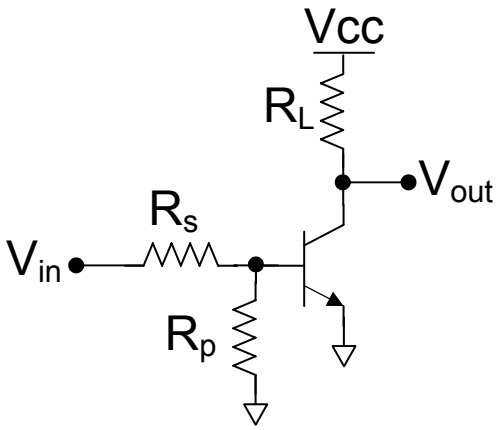



Figure 5.3: Simple LNA with resistive matching

### 5.1.2 A Simple LNA

The simplest form of an LNA is that shown in Figure 5.3, where a single common emitter amplifier is employed with resistive matching. In reality, however, this circuit suffers from many drawbacks. Foremost the use of resistive matching, while capable of providing a consistent 50 Ω match, contributes substantial thermal noise to the circuit. Considering that the parallel matching resistor acts as a voltage divider, where the maximum power is delivered to the base of the transistor when $R_s = R_p$, one might be inclined to set $R_p$ = 50 Ω. However doing so raises the minimum noise figure to 3 dB, as determined in equation 5.1.5 [30]:

$$NF = 10\log\left(1+\frac{R_s}{R_p}\right) = 10\log(2) \approx 3dB \tag{5.1.5}$$

This condition therefore requires that the parallel input resistance be very high, mandating alternate methods for creating a 50 Ω input match (using inductive and capacitive elements).

Before addressing using imaginary components for input (or output) matching, it is necessary to explore the frequency dependence of the device being employed. A simplified model of a common-emitter amplifier is shown in Figure 5.4.

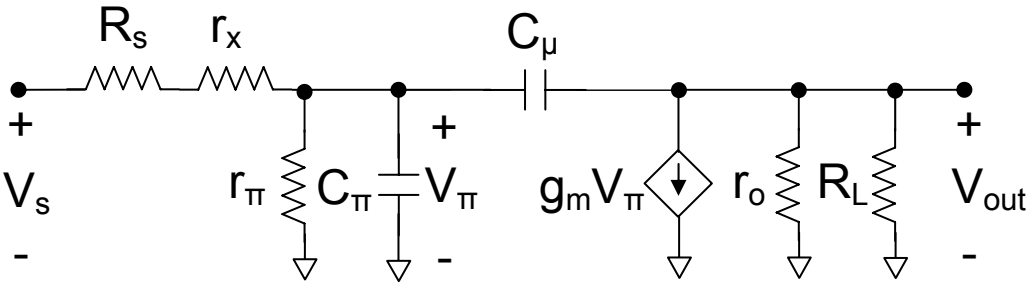



Figure 5.4: Simplified model of a common-emitter amplifier

In Figure 5.4 we have introduced two capacitors which will limit the bandwidth at high frequencies. $C_\pi$, which will shunt input power to ground at high frequencies, and $C_\mu$, which introduces feedback at high frequencies. Since the voltage gain at the output node is $V_{our}$=-gmVπ(ro$\|R_L$), we get a multiplication factor applied to the capacitance $C_\mu$, determined by the voltage ratio at either side of the capacitor. Using that the miller capacitance ($C_\mu$) can be rewritten as [31]:

$$C_{eq} = C_{\mu}\left(1 + g_m\left(\frac{r_o R_L}{r_o + R_L}\right)\right) \tag{5.1.6}$$

Which is an input referred effective shunt capacitance. From this the 3 dB roll-off frequency can be derived from the parallel combination of $C_{eq}$ and $C_{\pi}$ to be (assuming $r_{\pi}$ is large):

$$\omega_{3dB} = \frac{1}{(R_s + r_x)(C_{\pi} + C_{eq})} \tag{5.1.7}$$

Equation 5.1.7 shows that while $C_{\mu}$ is typically quite small, it can have a very large impact on the bandwidth of the systems due to the exaggeration of its effect caused by the voltage imbalance across it. As such efforts taken to mitigate this effect (by reducing the effective load resistance) are often employed, especially cascoded topologies. While Cπ also has a limiting effect on the bandwidth, it is often useful in matching the input of a common-emitter amplifier, as will be shown later through emitter degeneration.

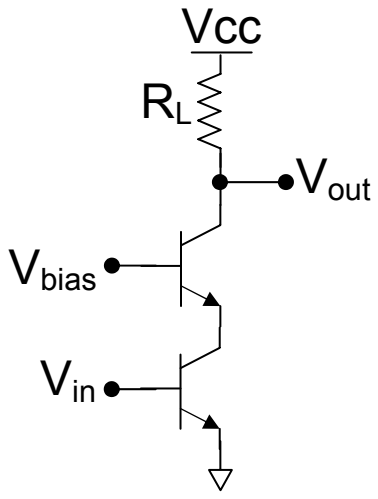



Figure 5.5: Basic cascode topology

## 5.2 Cascode Topologies

In the cascoded amplifier shown in Figure 5.5 the common-emitter amplifier has been modified by introducing a common base stage between its collector and the load, $R_L$ [9]. This topology has many benefits over the conventional common-emitter amplifier, including increased gain and improved reverse isolation, but it's greatest contribution is the degradation of the effects of the miller capacitance (of the common-emitter stage) [32]. In the previous analysis of the miller capacitance it was observed that effective input referred capacitance was determined by the load resistance, $R_L$. By introducing a cascode the load resistance is replaced with the input resistance of the common-base stage, $r_e$. Since $r_e$ is much less than the load resistance (typically) the effective input referred capacitance is very close to the miller capacitance, which is typically quite small. Another way of analyzing this is considering that the collector-emitter junction between the input and cascode stages is largely current mode, and therefore does not support the voltage differential that causes the multiplication factor of the miller capacitance. Also, since the current swing through the cascode is approximately the same as that through the input stage ($g_m v_\pi$ vs. $\alpha g_m v_\pi$), the output load of the amplifier can be much larger than $r_o$, instead becoming $r_o(1+g_m r_\pi)$. From this a new gain relationship can be written as:

$$\frac{V_{out}}{V_{in}} = -\alpha g_m V_\pi \left( \frac{r_o(1+g_m r_\pi)R_L}{r_0(1+g_m r_\pi)+R_L} \right) \tag{5.2.1}$$

Which, assuming $r_o(1+g_m r_\pi) >> R_L$, is approximately $\alpha(1+g_m r_\pi)$ greater than the common-emitter amplifier.

Beyond these benefits, there are certain disadvantageous to cascoded LNAs. Foremost, the added device doubles the headroom required for such a topology, making them problematic for low voltage design (and therefore low power). Also, the additional transistor increases the number of noise sources in the circuit, although this drawback is typically compensated by the increased isolation of later noise stages due to the higher gain. Also, cascode amplifiers typically suffer from impaired linearity vs. a common-emitter amplifier, which might be detrimental if the LNA needs to accommodate a large dynamic range (which is more likely at high frequencies due to the higher attenuation rates in the atmosphere).

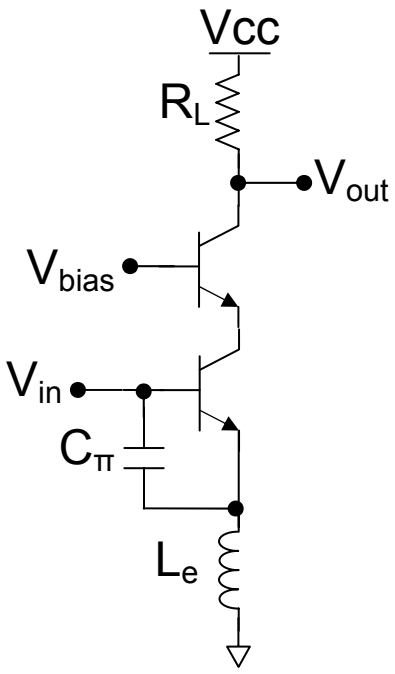



Figure 5.6: Inductively degenerated LNA

## 5.3 Emitter Degeneration

As was mentioned previously the base-emitter capacitance $c_\pi$ can be used in conjunction with emitter degeneration to create a 50 Ω (or other) match at high frequencies [30]. The primary function of emitter degeneration, as it applies to LNAs, is to create a real input impedance at the base of the transistor. An example of this type of degeneration can be seen in Figure 5.6. From Figure 5.6 the input impedance can be written as:

$$Z_{in} = r_b + \frac{g_m L_e}{C_\pi} + L_e s + \frac{1}{C_\pi s} \tag{5.3.1}$$

Where $L_e$ and $C_\pi$ can be chosen to set $Z_{in}$ = 50 Ω. Note that in reality that this isn't always obtainable, or optimally, so $L_e$ and $C_\pi$ might simply act to make the impedance real, with external matching applied to satisfy the 50 Ω requirement. Also note that much of the manipulation will occur to $L_e$, since the device size (and therefore $C_\pi$) are typically chosen to minimize noise. The capacitance $C_\pi$ can be externally manipulated using a discrete capacitor; however that is typically not advantageous for high frequency design.

There are, however, certain drawbacks to inductive degeneration. Foremost, beyond creating a real input impedance the degeneration inductor acts to lower the Gm of the input stage, limiting the gain and thereby inhibiting the LNAs ability to isolate successive noise stages (or, of the cascode device). This effect of inductor degeneration can be seen in equation 5.3.2.

$$\frac{V_{out}}{V_{in}} = g_m s L_e \left( \frac{1}{1 + g_m s L_e} \right) \tag{5.3.2}$$

Another drawback of inductive degeneration is the size of the inductor required, which can increase substantially the size of the LNA.

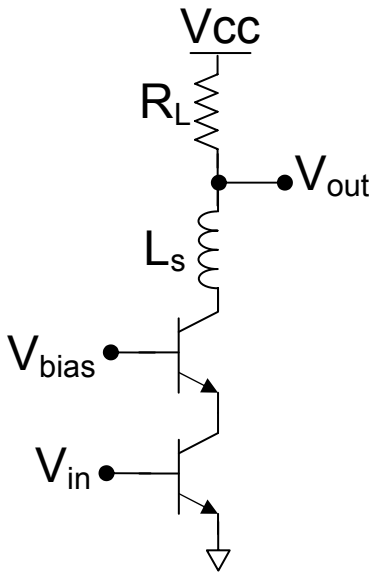



Figure 5.7: LNA with series-shunt matching

## *5.4 Series-Shunt Output Matching*

While input matching was discussed in section 5.3, output matching requires further analysis. Similar to the base of a transistor, the collector of a transistor is subject to a capacitance $C_\mu$. The effect of this capacitance is to restrict the bandwidth at the output node. Considering the cascode topology described in section 5.2, the impedance at the output port is:

$$Z_{in} = \frac{R_L}{1 + sR_L C_\mu} \tag{5.4.1}$$

Where the load resistance and Miller capacitance form a low pass filter with a pole at $1/(R_L C_\mu)$. A modification to the cascoded LNA can be seen in Figure 4.7, where an

inductor is added in series with the collector [33]. From this circuit a new output impedance can be derived as:

$$Z_{in} = \frac{R_L\left(s^2 L_s C_\mu + 1\right)}{s^2 L_s C_\mu + sR_L C_\mu + 1} \tag{5.4.2}$$

Where a zero has been introduced at $s = \sqrt{(L_s C_\mu)}$. While this technique also introduces an added pole, careful sizing of the inductor will allow for increased bandwidth in the output matching impedance. Alternatively the inductor can be thought of resonating with the Miller capacitance to generate a high impedance from $V_{out}$ to the collector as the capacitor acts to shunt AC output power. Assuming negligible losses in the inductor, this technique does not inhibit output power and gain, as the same current swing will be experienced at both ends of the inductor (in fact, by increasing the bandwidth of the match this technique actually improves the gain of the circuit).

This technique is not without it's drawbacks, however. While the inductor creates a large input impedance looking into the collector of the transistor, it also creates a large input impedance looking out of the collector, which can amplify the Miller effect in the cascode. While typically this effect would be insignificant, since the cascode is in common-base configuration, if the DC bias node isn't a suitable AC ground the feedback can drive it as a common-emitter, potentially introducing instability. This becomes all the more crucial at the high frequencies as the low capacitance density in silicon technologies makes it impossible to have a perfect AC ground. Also, this technique does introduce some physical area to the design, but as it is largely useful at high frequencies the series inductance is usually realized with a small segment of transmission line.

Note that while this analysis (and all others in this chapter) were done employing a resistive load, the same principles hold if an inductive load is employed to provide only a narrowband match.

## 5.5 Balun Operations

Most wireless receivers employ single ended antennas, thereby requiring a single ended input to the LNA. Despite that, many receivers are designed for differential operation, reaping the benefits of improved tolerance to supply fluctuations, better common-mode rejection, and less sensitivity to substrate noise effects. To accommodate this requirement, it is necessary to convert the single ended single into a differential signal in the early stages of the receiver. To that end two methods can be employed, either using a passive balun or an active balun. The advantage of a passive balun is good phase separation with no power consumption, however since it is lossy it degrades the noise figure of the system. Also, since passive baluns are typically half wavelength in scale they can be quite large even at mmWave frequencies. By employing an active balun, which can provide gain, the circuit can achieve single-ended to differential operation while also providing gain, thereby potentially improving the total receiver noise figure. Another benefit of an active balun configuration is that it can operate at low frequencies without being unwieldy in size, and can potentially have more bandwidth than a passive LNA.

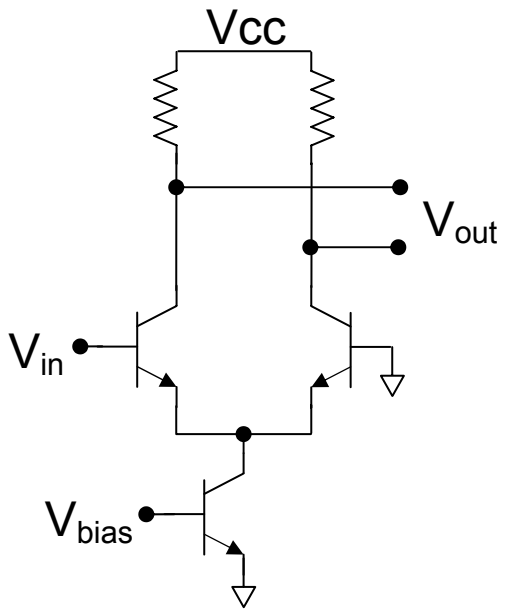



Figure 5.8: Emitter coupled pair employed as a Balun

The simplest form of active balun can be seen in Figure 5.8, where one port of an emitter coupled pair is driven by the single ended signal and the other is tied to a fixed bias point (AC ground) [9]. This circuit operates by sharing the AC current of the input device between the two halves of the emitter coupled pair (in that regard it can also be thought of as a common emitter amplifier in parallel with a common base amplifier), therefore driving a differential current across the two load resistors.

The behavior of this balun can be realized by observing that the tail current source has high input impedance, suppressing AC current flow. That requires that the AC path flows through both half of the emitter coupled pair, so the current swing through the differential path will track the current swing through the in phase path (less any losses through the tail current source, due largely to finite impedance caused by $C_\mu$ and $C_\pi$). The phase difference between the two can be derived from the solution to KCL at the common (coupled) node. As one half of the emitter coupled pair is

driven with the input voltage $V_{in}$, it will draw a certain current from the current source. As this occurs, the other half of the pair must consume the rest of the current. In doing so, as the voltage $V_{in}$ swings higher (and draws more current), the current through the other device will be driven lower (and vice versa). This behavior causes the differential behavior of the output, as the current is alternately split across the two devices (note that unless the input voltage swing is large enough to completely saturate, and alternately cutoff the device some current will always be carried through each transistor).

Another incarnation of the active balun again uses an emitter coupled pair, although here the tail current is replaced with an LC tank, as shown in Figure 5.9. Employing a tank relaxes the headroom constraint present with an active tail current, although does so with certain risks. By resonating the tail current at the common mode frequency of the balun it can achieve the same high impedance operation as the active current source, although that impedance profile is narrow band. The quality of the tank also plays a large role, as a high Q tank would be ideal for creating a high impedance common mode termination, although it will make the balun more narrow band in operation. Another drawback of this topology is the area occupied by the tank. This is especially a concern at high frequencies since increased circuit size increases the amount of necessary wiring, increasing the potential for unwanted parasitics.

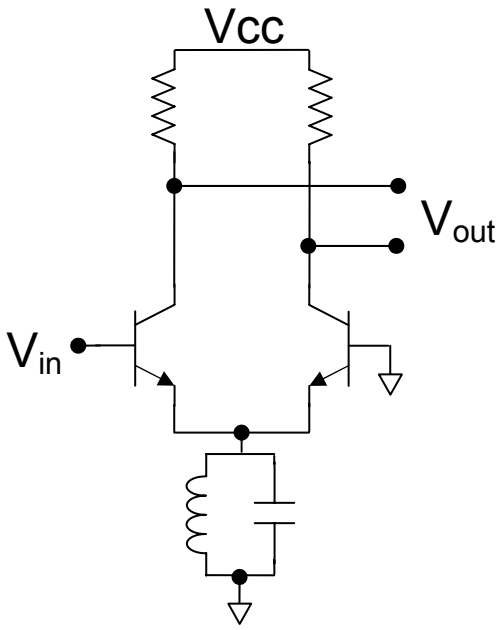



Figure 5.9: LC tank degenerated emitter coupled pair employed as a Balun

# Chapter 6 LNA Design Examples

## *6.1 A 20 GHz SiGe LNA*

A 20 GHz low noise amplifier (LNA) with an active balun fabricated in a 0.25 μm SiGe BICMOS ($f_t$ = 47 GHz) technology was presented in [34,35]. The LNA achieves close to 7 dB of gain and a noise figure of 4.9 dB with all ports simultaneously matched to 50 Ω with better than –16 dB of return loss. The amplifier is highly linear with an $IP_{1dB}$ of 0 dBm and $IIP_3$ of 9 dBm, while consuming 14 mA of quiescent current from a 3.3V rail, with temperature compensated biasing. At the time of development the LNA delivered the lowest noise figure of any LNA in the 20 GHz range, and is the first implementation of an active balun employing an LC degenerated emitter coupled pair.

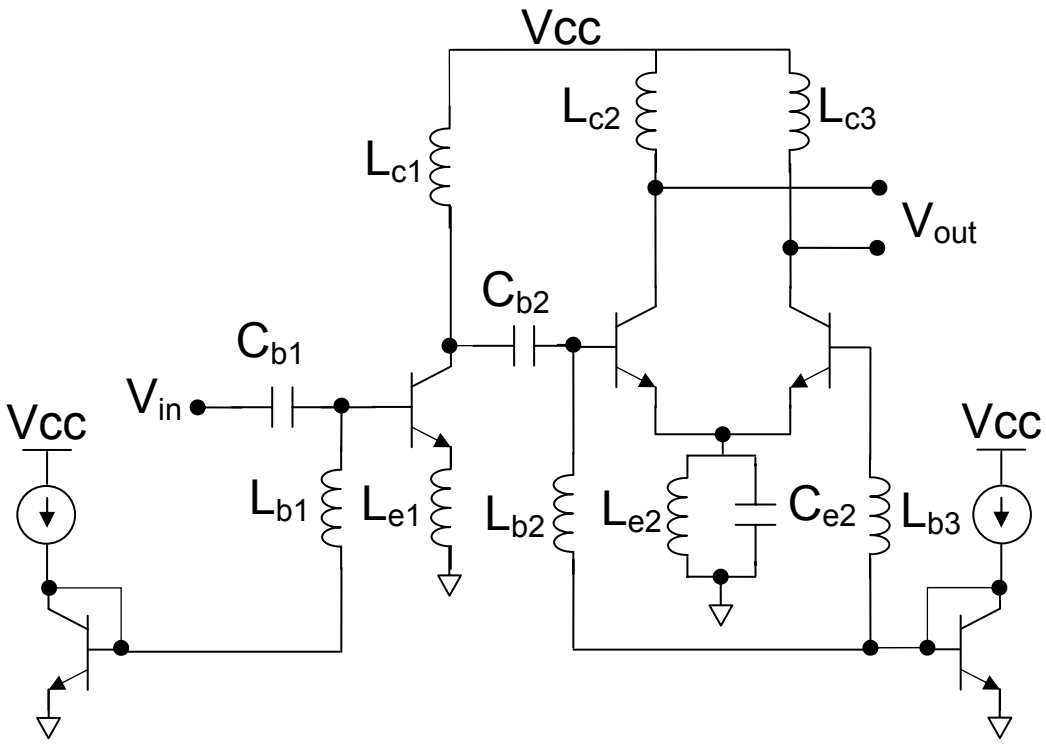



Figure 6.1: LC degenerated active balun

### 6.1.1 LNA Design

A simplified schematic of the two stage LNA is shown in Figure 6.1. The input stage is a single-ended common-emitter amplifier with a temperature compensated voltage bias applied across the base-emitter junction. Due to the additional noise component of the following balun stage (due to the parallel branches of the emitter-coupled pair) it becomes increasingly necessary to mitigate the noise effects of the first stage. These noise effects place certain restrictions on the available device sizes for the design, which is complicated further by the high frequency operation of the LNA, which requires that all transistors be biased at (or near) maximum $f_t$. To mitigate thermal noise effects of the base contact a multiplicity of smaller devices is favored over a single larger device, limiting the base resistance and ensuring more uniform current distribution across the device.

Input matching is achieved with a small emitter degeneration inductor $L_{e1}$, and the resonant circuit created by the inductor $L_{b1}$ and the DC blocking cap $C_{b1}$. The input impedance can be expressed as (assuming a negligible miller effect) [15]:

$$Z_{in} = \frac{L_{b1}s\left(r_b + g_m L_{e1}/C_\pi\right)}{L_{b1}s + r_b + g_m L_{e1}/C_\pi} + \frac{1}{C_{b1}s} \tag{6.1.1}$$

Since it is desired to minimize $g_m$ and $r_b$ to reduce the noise contribution of the leading stage, a larger degeneration inductance $L_e$ is required to transform the input impedance to 50 Ω. The larger degeneration inductance will decrease the voltage gain of the stage, however, as was predicted in equation 5.3.2.

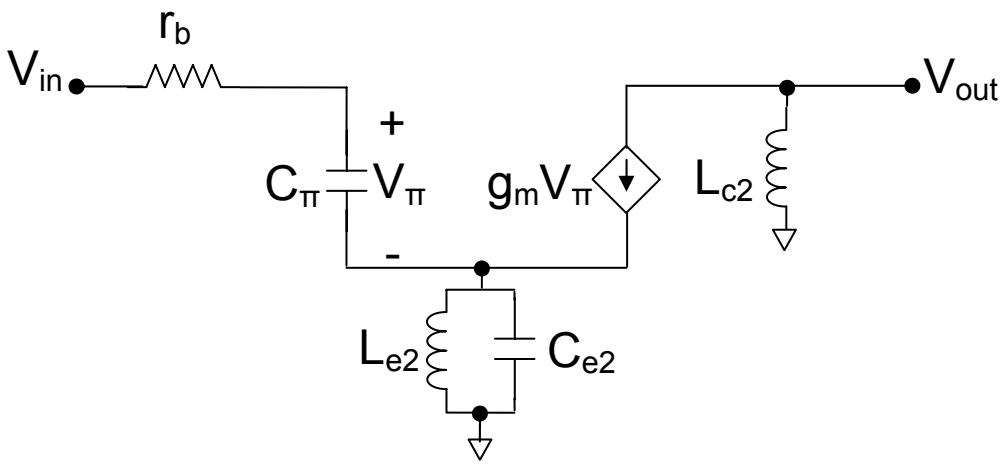



Figure 6.2: Simplified emitter coupled pair small signal model

The second stage is an emitter coupled pair degenerated with an LC tank (created by $L_{e2}$ and $C_{e2}$) optimized to resonate at twice the target operating frequency (40 GHz) to reject the common mode at the emitters. Neglecting the differential half of the emitter coupled pair we can draw the small signal model shown in Figure 6.2. Using this model the input impedance of the second stage is [15]:

$$Z_{in} = \frac{L_{b2}s\left(r_b + \frac{g_m C_{e2}}{C_\pi}\left(\frac{1+L_{e2}s}{C_{e2}s+L_{e2}s}\right)\right)}{L_{b2}s + r_b + \frac{g_m C_{e1}}{C_\pi}\left(\frac{1+L_{e2}s}{C_{e2}s+L_{e2}s}\right)} + \frac{1}{C_{b2}s} \tag{6.1.2}$$

Assuming that the AC base current is small (and $C_\pi$ is negligible) the second stage transfer function is:

$$\frac{V_{out}}{V_{in}} = g_m sL_{c2}\left(\frac{1+s^2 C_{e2}L_{e2}}{1+s^2 C_{e2}L_{e2} + g_m sL_{e2}}\right) \tag{6.1.3}$$

In this circuit an inductor was added to the base of the differential half of the active balun, even despite previous efforts showing that it wasn't required. The purpose of the additional inductor is to mimic the loading effects of the first stage to allow for an improved, and similar, output match of the in-phase and differential ports.

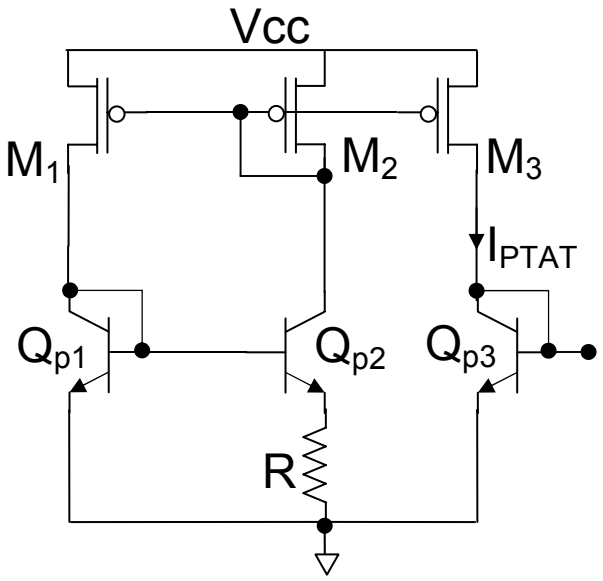



Figure 6.3: PTAT bias circuit

In Figure 6.3 the PTAT bias network of the LNA can be seen, which is applied to both stages of the circuit. The PTAT uses a half degenerated HBT current mirror driven by a PFET mirror to generate a temperature dependent current of [36]:

$$I_{ptat} = \frac{V_t}{R} \ln\left(\frac{W_{Qp2}}{W_{Qp1}}\right) \tag{6.1.4}$$

### 6.1.2 Layout Considerations

Careful consideration during layout was required to ensure minimal and comparable parasitics throughout the LNA. The second and third stages were oriented symmetrically about the horizontal axis, with the exception of variations in the size of matching inductors $L_{b2}$ and $L_{b3}$. All matching was done on chip with strait wire inductive lines used to allow for large spacing between the inductors to improve isolation, shielded with a DC ground at a distance of 80 µm to provide a local current return path (without introducing excess parasitic capacitance). Interstage 50 Ω transmission lines were used to minimize the amount of non-modeled wiring, and banks of decoupling capacitors were located at the termination of each inductor (and the collectors of the two emitter followers) to provide good local AC return paths (50 Ω pads and wiring were also used for DC connections in the test environment to mitigate power supply resonances).

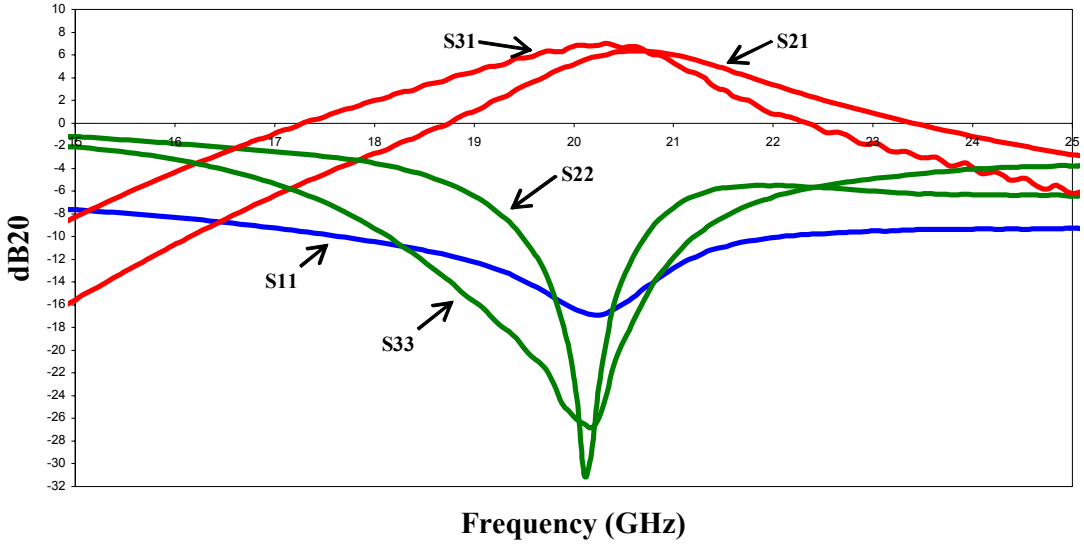



Figure 6.4: LNA Small Signal S-Parameters

### 6.1.3 Experimental Results

Figure 5.4 shows the small signal S-parameters for the LNA with active balun, where $S_{21}$ is 6.31 dB and $S_{31}$ is 6.7 dB at 20.5 GHz. These measurements indicate a better than –16 dB of return loss at the input port and better than – 26 dB of return loss at each of the output ports.

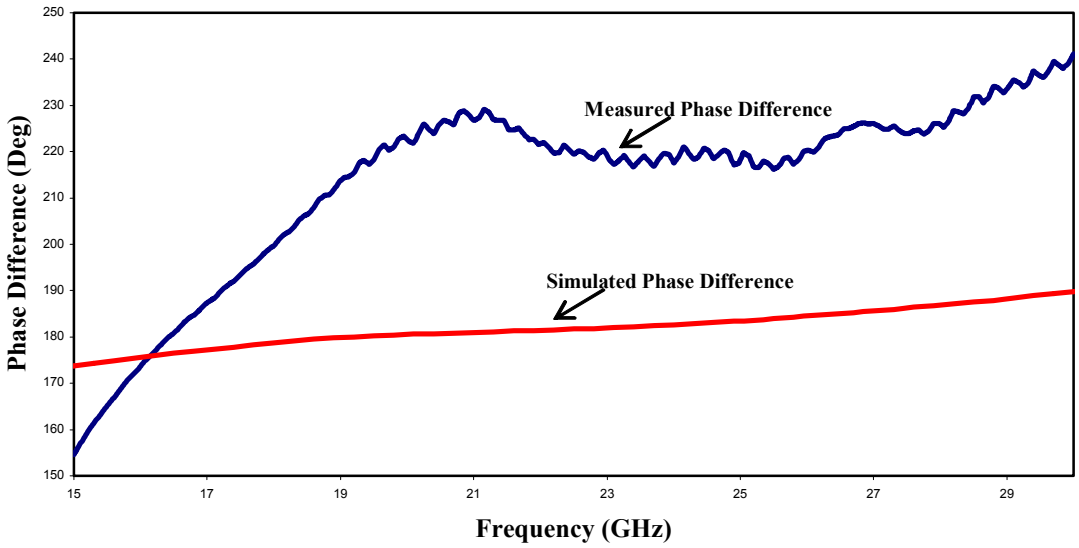



Figure 6.5: LNA Measured and Simulated Phase Separation

Figure 6.5 depicts the simulated and measured differential output phases. There is a 39° disparity in the simulated and measured results for the output phases of the two paths at 20GHz. Since only two port small-signal measurements were possible and each data set required a separate calibration (the output port connection had to be moved between the two signal pads of the G-S-G-S-G probe, requiring the probes to be removed from the IC), exact phase testing was not possible (also, phase shifters

were not available to compensate for deviations in the electrical length of the cable/adapter/probe assembly). There may also be variations in the rejection frequency of the tank in the emitter-coupled pair due to unmodeled parasitics, which would introduce another AC current path at the frequency of interest. Without having access to a four-port network analyzer achieving a highly accurate phase measurement would be difficult, but even without doing so we can see that the use of an LC tank within the emitter-coupled pair is sufficient for creating two distinct and separate phases.

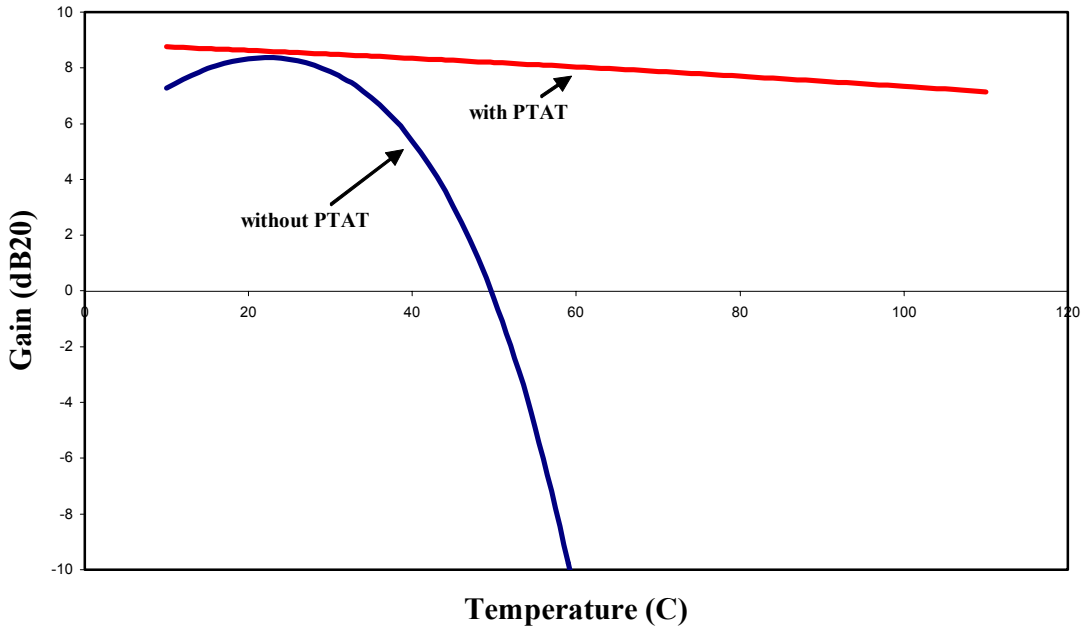



Figure 6.6: Simulated LNA Gain vs. Temperature with and without PTAT

The effect of the PTAT biasing on the in-phase and differential gain of the circuit is shown in Figure 6.6. From this figure, it is evident that employing two stages of PTAT biasing stabilizes the gain to about 2 dB/ 100° C of variation, whereas a

fixed bias point causes the gain to drop off very rapidly above 23° C, dropping below unity at 50° C.

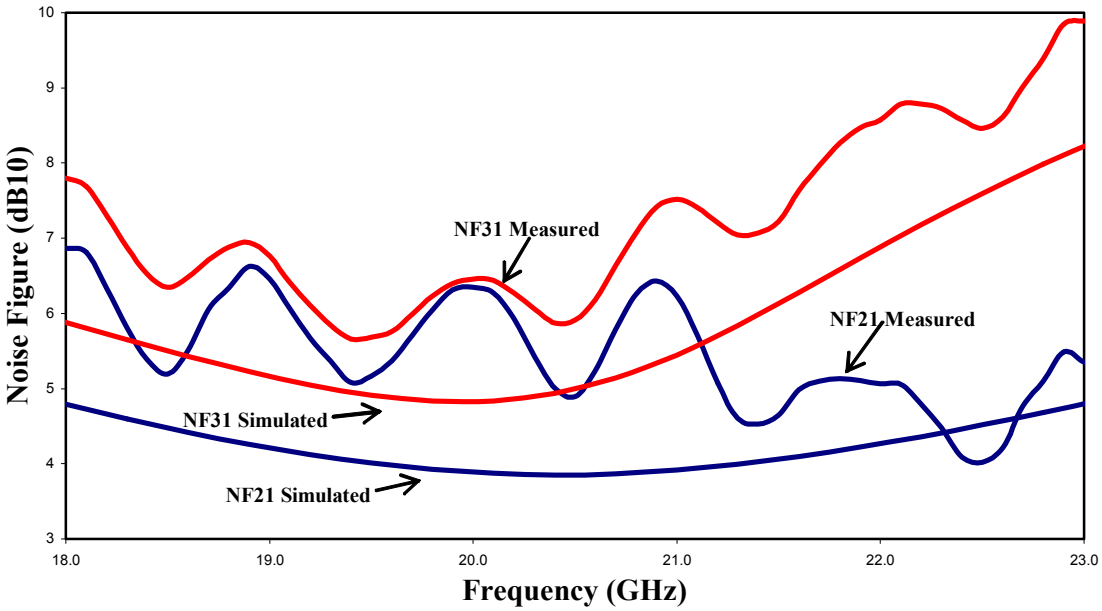



Figure 6.7: LNA Measured and Simulated Noise Figures

Measured and simulated noise figures of the LNA are shown in Figure 6.7. At 20.5 GHz output port 2 yields a noise figure of 4.89 dB ($NF_{21}$) while $NF_{31}$ is 5.91 dB. $NF_{21}$ is the lowest reported value at 20 GHz for a silicon LNA. The simulated noise figures are included to show the general shape of the curves (some rippling was introduced during testing due to ENR limitations of the test equipment), and to emphasize that the difference between the noise figures ($NF_{21}$ & $NF_{31}$) remained about 1 dB (showing that the symmetrical layout style introduced the same parasitic effects to each path). This difference is to be expected due to the manner in which the two halves of the emitter-coupled pair are driven, with the in-phase branch driven as a

common-emitter amplifier and the differential path driven as a common-base amplifier (thus incurring a slightly greater noise for an identical device size [37]).

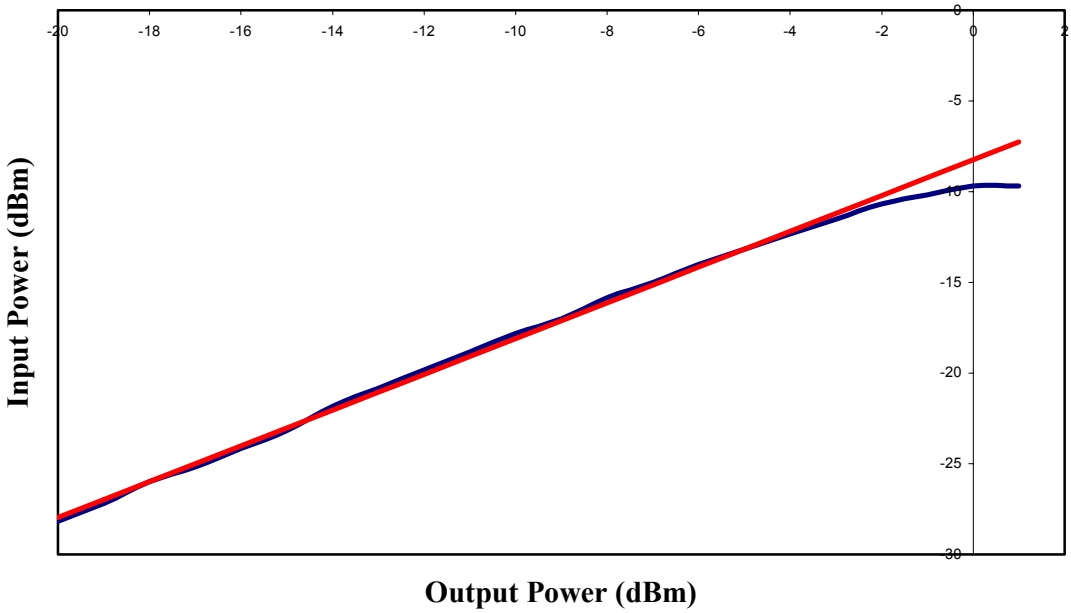



Figure 6.8: LNA Input Referred 1dB Compression

Figures 6.8 and 6.9 demonstrate that the LNA is highly linear, with an input referred 1dB compression point of 0 dBm and an input referred IP3 of 9 dBm (extrapolated from –5 dBm input power). These measurements were observed while drawing 14 mA of quiescent current from a 3.3 V rail, for a total power consumption of 46.2 mW. The chip microphotograph is shown in Figure 5.10. A summary of the LNA performance can be seen in Table 6.1, with comparison to other works in Table 6.2.

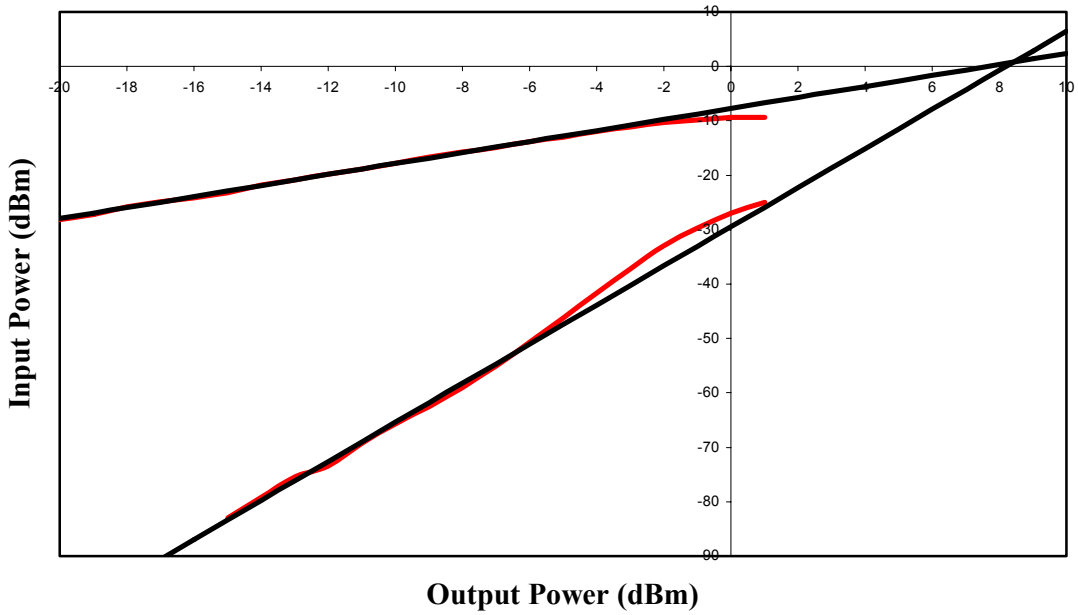



Figure 6.9: LNA Input Referred IP3

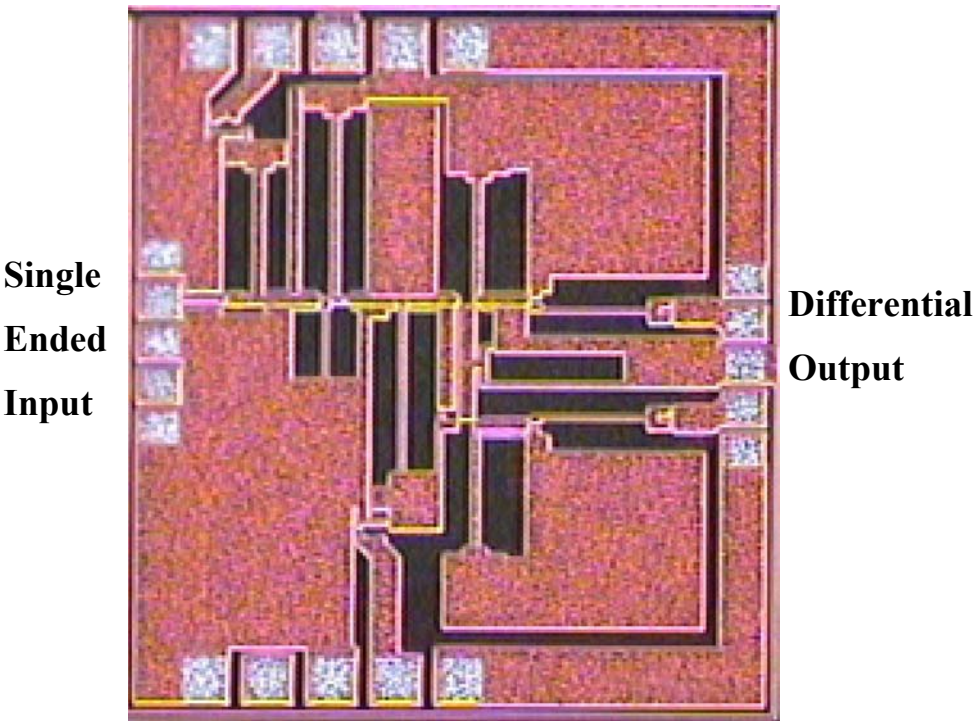



Figure 6.10: LNA Die Photo

Table 6.1: Comparison of 20 GHz LNA Performance to Published Works

| | | | |
|---|---|---|---|
| Frequency | 20.5 GHz | NF2 | 4.89 dB |
| S21 | 6.31 dB | NF3 | 5.91 dB |
| S31 | 6.7 dB | P1dB | 0 dBm |
| S11 | -16.9 dB | IIP3 | 9 dBm |
| S22 | -26.8 dB | Supply | 3.3V |
| S33 | -31 dB | DC Current | 14 mA |
| Phase Delta | 219° | | |

Table 6.2: Summary of 20 GHz LNA Performance

| | Feature Size | Technology | Balun | Frequency | Gain | NF | Power |
|---|---|---|---|---|---|---|---|
| LNA in [38] | 0.18 μm (ft =45 GHz) | Bulk Si | No | 24 GHz | 12.86 dB | 5.6 dB | 54 mW |
| LNA in [39] | 0.10 μm (ft =95 GHz) | SOI | No | 23.8 GHz | 7.3 dB | 10 dB | 79 mW |
| LNA in [40] | 0.18 μm | Bulk Si | No | 24 GHz | 15 dB | 6 dB | 24 mW |
| This Work | 0.25 μm (ft=47 GHz) | SiGe | Yes | 20.5 GHz | 6.9 dB | 4.89 dB | 46 mW |

## *6.2 A 24 GHz CMOS LNA*

Complimentary to the 20 GHz SiGe LNA a 24 GHz LNA has been designed using a 0.13 μm CMOS technology (CMRF8SF). The amplifier achieves up to 16 dB of Gain with a noise figure of 7.4 dB, while outputting differential signals with less than 5º phase error. In this design Balun operation is also achieved, using a similar topology to the SiGe LNA, but with the addition of certain techniques as described in chapter 5. Among these are amplifier cascoding and series-shunt matching.

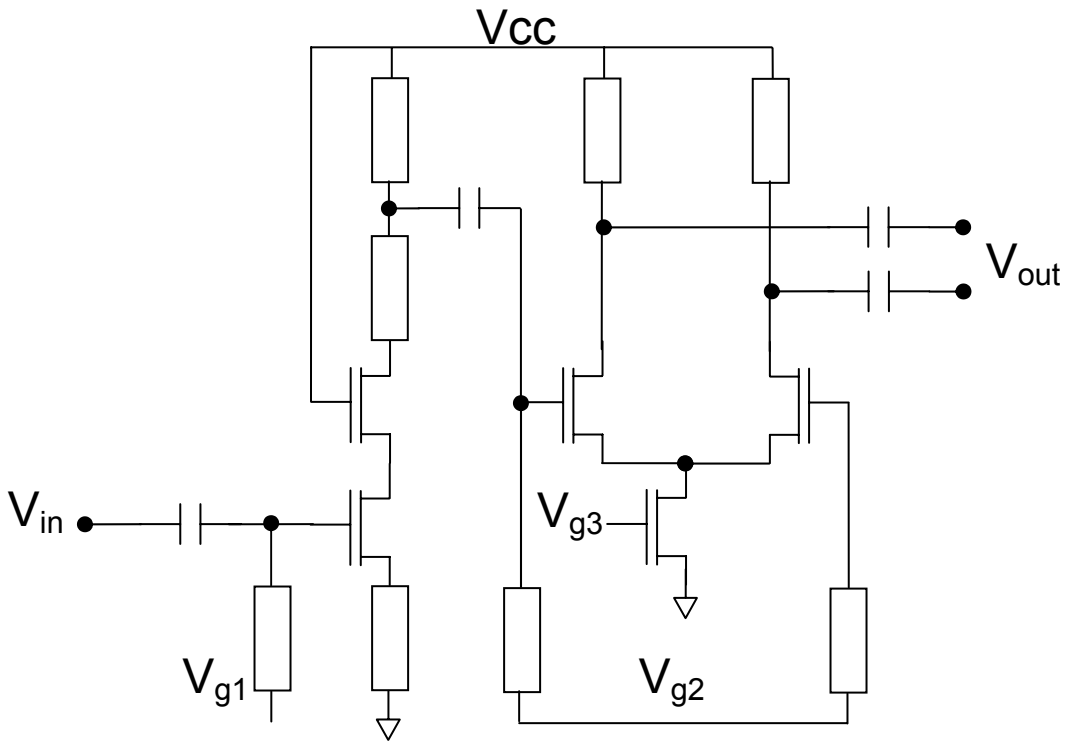



Figure 6.11: 24 GHz CMOS LNA with Active Balun

### 6.2.1 LNA Design

A schematic of the 24 GHz CMOS LNA can be seen in Figure 6.11, sans bias circuitry. Again a two stage topology is employed where the first stage is a single ended low noise stage driving an emitter coupled pair. By using transmission line type matching and an advanced CMOS technology several techniques can be employed that where previously impossible in the SiGe technology used in the LNA described in section 6.1. The low headroom (and high $f_t$) of the CMOS devices allows them to be double stacked, enabling cascoding of the input stage and a differential pair source coupled over an active current source. While the cascode mitigates the effects of the miller capacitance of the common-source stage, an equally larger benefit is realized by

using a proper source coupled pair. In doing many of the unknown parasitics that afflicted the common-emitter pair from the SiGe LNA are eliminated, preventing phase mismatches at the output. Also, the series-shunt output matching of the first stage enables the first stage to drive a greater voltage swing to the second stage, increasing the circuits gain.

Despite the benefits of this technology (benefits that are also present using more advanced SiGe technologies), there are certain hurdles to the design process. Device linearity and gain can be a factor under high input powers, although that concern is less dire in a low noise amplifier. The greatest limitation of a CMOS device is the high (relative to SiGe) gate impedance of the transistors, which makes conjugate matching more difficult. Using the source degenerated topology from the first stage the input impedance can be derived to be [30]:

$$Z_{in} \approx \frac{g_m L_s}{C_{gs}} + L_s s + \frac{1}{C_{gs} s} \tag{6.2.1}$$

Where $L_s$ is the degeneration inductance and $C_{gs}$ is the gate-source capacitance of the input device. This equation is similar to that described in equation 5.3.1, except without the effect of the series base resistance of the HBT, which helps achieve a real input impedance. As such this requires more exact balancing between the degeneration inductance and gate-source capacitance to create a real input impedance, typically much greater than 50 Ω. Since the available real input impedance for a degenerated CMOS device is much higher than for a degenerated HBT, more external matching elements are typically required to achieve a 50 Ω input match. This requirement for additional matching circuitry degrades (potentially) the circuit in two ways, by

restricting the input matching bandwidth (although this may actually be a benefit) and by introducing sources of variability.

Biasing for the circuit is provided through the simple bias network shown in Figure 6.12, where an external override bias voltage can be applied across the PFET current mirror. This network was chosen due to its low power consumption and low sensitivity to noise on the DC bias nodes.

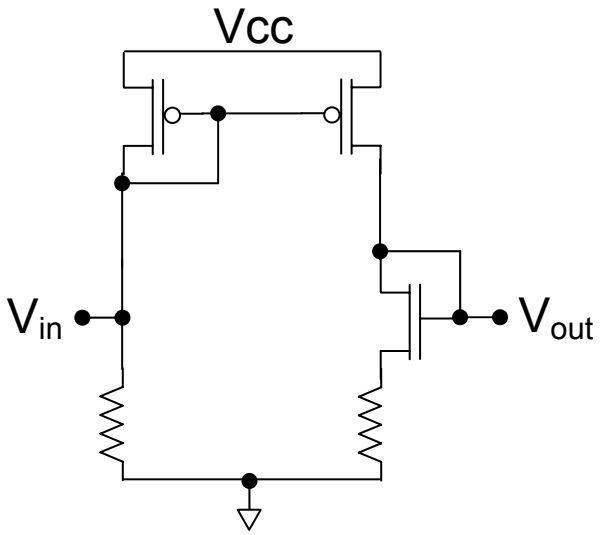



Figure 6.12: Simple LNA Bias Network

### 6.2.2 Layout Considerations

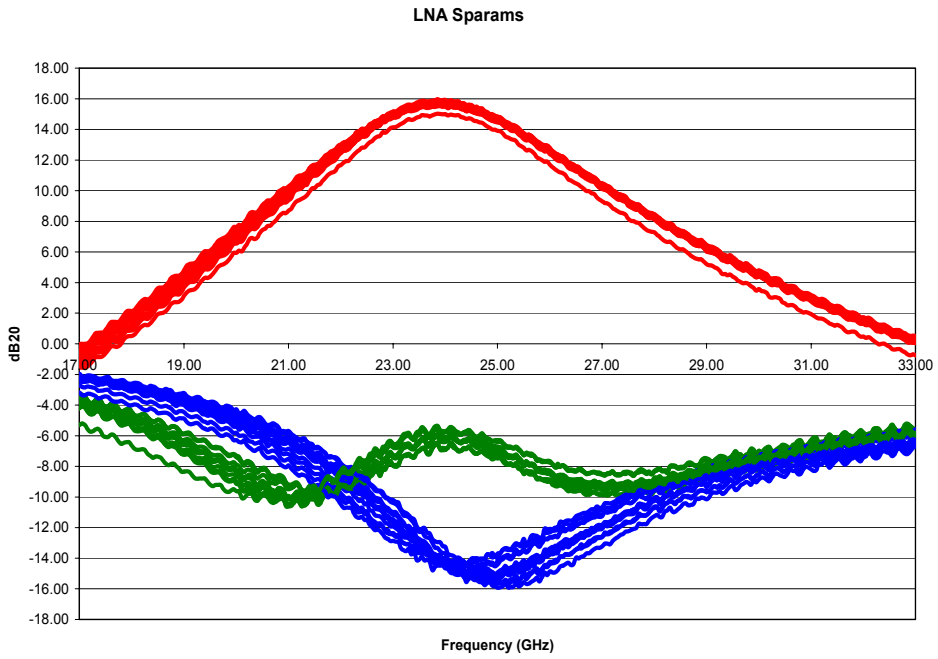
By using a transmission line based matching methodology significant improvements in layout were achieved over the previous LNA. The ability to bend the transmission lines (and their relatively long lengths) ensured accurate common mode placements in the second stage, minimizing the effects of imperfect power distribution. This ability was also aided by replacing the LC tank in the previous differential pair with an active current source, which occupies considerably less area. By using shielded transmission lines the large spacing requirements between inductors

was relieved, eliminating the need for long runs of inter-stage wirings. One drawback of the CMOS technology was the lack of a small capacitor, creating the need to employ series capacitors at most of the AC coupling nodes, which introduced increased parasitic capacitances due to their large area. This wasn't exclusively a limitation of the available capacitors, but was also due to the extremely small capacitances needed to match to the high impedance CMOS devices.

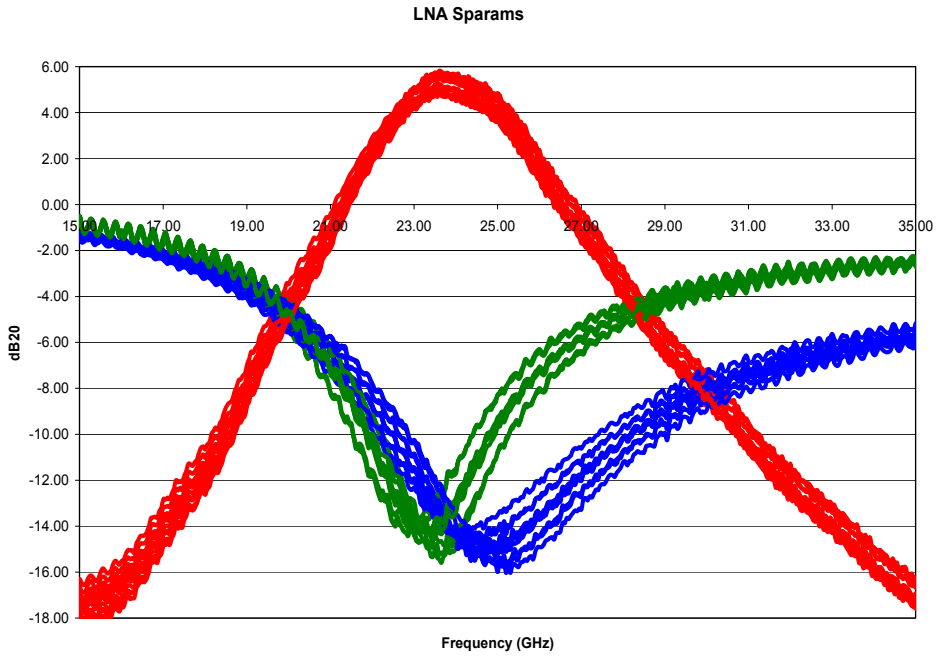
Another limitation of the CMOS technologies is their lack of a deep trench isolation structure, which is common in SiGe technologies. These structures are useful in disrupting substrate currents to isolate individual devices and circuits sharing a silicon platform, especially low frequency elements which are not absorbed by decoupling capacitance in the power structure. This limitation places more stringent demands on wiring near the substrate, which will become ever more challenging with increasing IC frequencies.

### 6.2.3 Experimental Results

Small signal s-parameters for the LNA can be seen in Figure 6.13, for both the in phase and differential port (families of curves are for different samples, with slight deviations to the matching networks). The in phase port shows remarkable performance and good matching, however there is serious degradation in the gain of the differential path.




(a)




(b)

Figure 6.13: Small Signal S-Parameters for the (a) In Phase and (b) Differential Paths

While the exact cause of the degradation to differential path is unknown, several culprits can be identified as likely causes. While typically a differential pair is configured to act as a Balun by affixing the unused input port to a fixed DC bias (AC ground), here the biasing is provided across a transmission line to control the output match of the device (attempt to mimic the loading effects of the first stage). While this does help the matching it may be detrimental to the gain and, as we will see, noise figure. Also, the output match of the differential path requires smaller capacitors to achieve 50 Ω, these smaller capacitors having fewer vias connecting the capacitor layer to the analog metal layers, which may incur significant losses. Notwithstanding these shortcomings the LNA displays exceptional phase separation, as demonstrated in Figure 6.14.

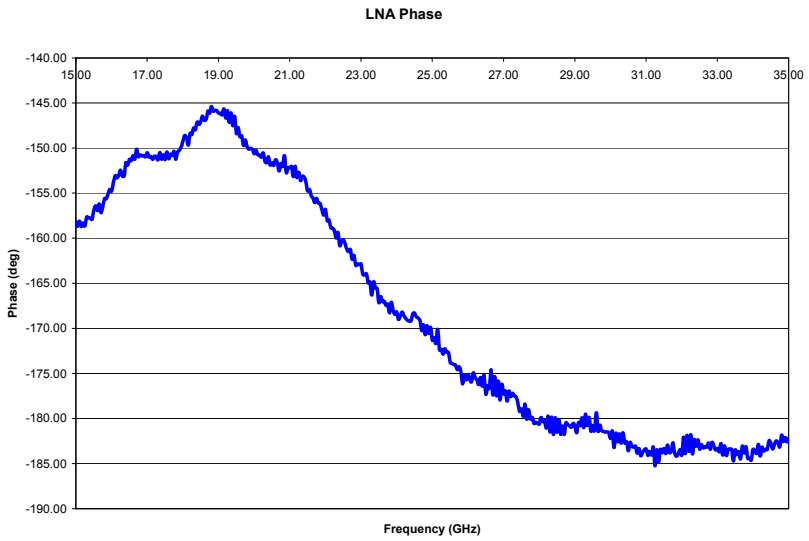



Figure 6.14: Phase Difference of the In-Phase and Differential Paths

The degradation in the differential path can also be seen in the noise figure plots of Figure 6.15. In this circuit the noise figure of the LNA is significantly higher than that of the SiGe version, although that is offset somewhat by the significantly

higher gain, which would further isolate the noise effects of later stages. The measured noise figure is also higher than the simulate noise figure ($NF_{min}$ = 4.5 dB), which can be attributed to input mismatches, poor device noise models (CMOS noise models typically are not verified to high frequencies), and calibration errors. Calibration errors can play an especially large role at higher frequencies as the losses referred to the input test structure can be as many as a few dB, even for just the probe.

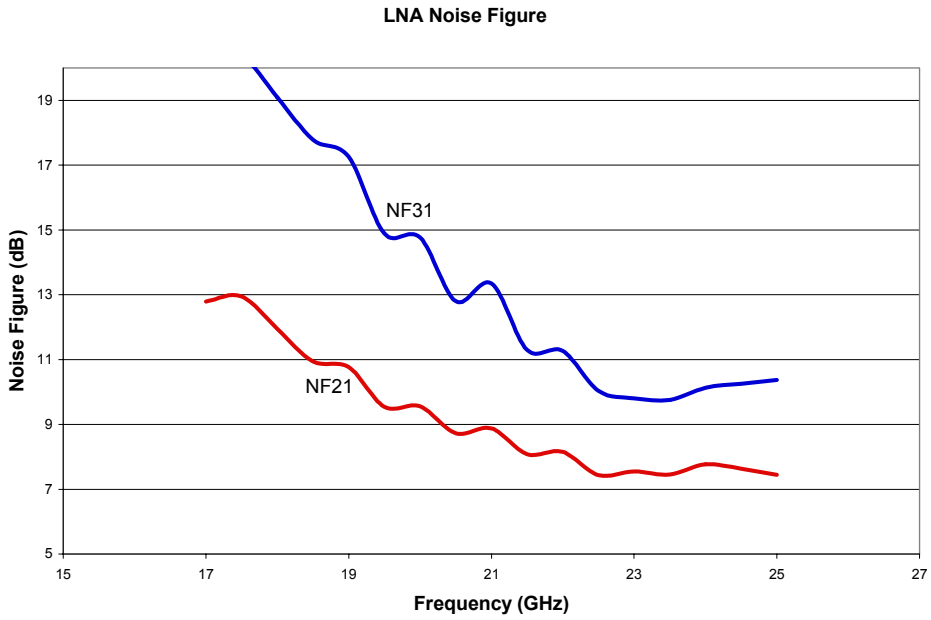
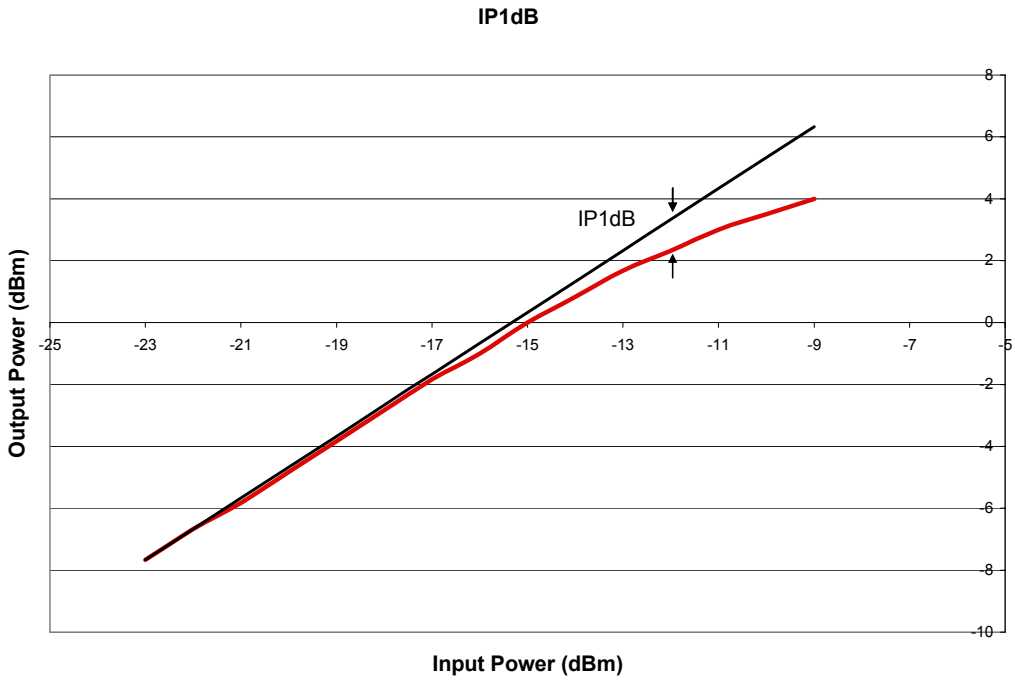
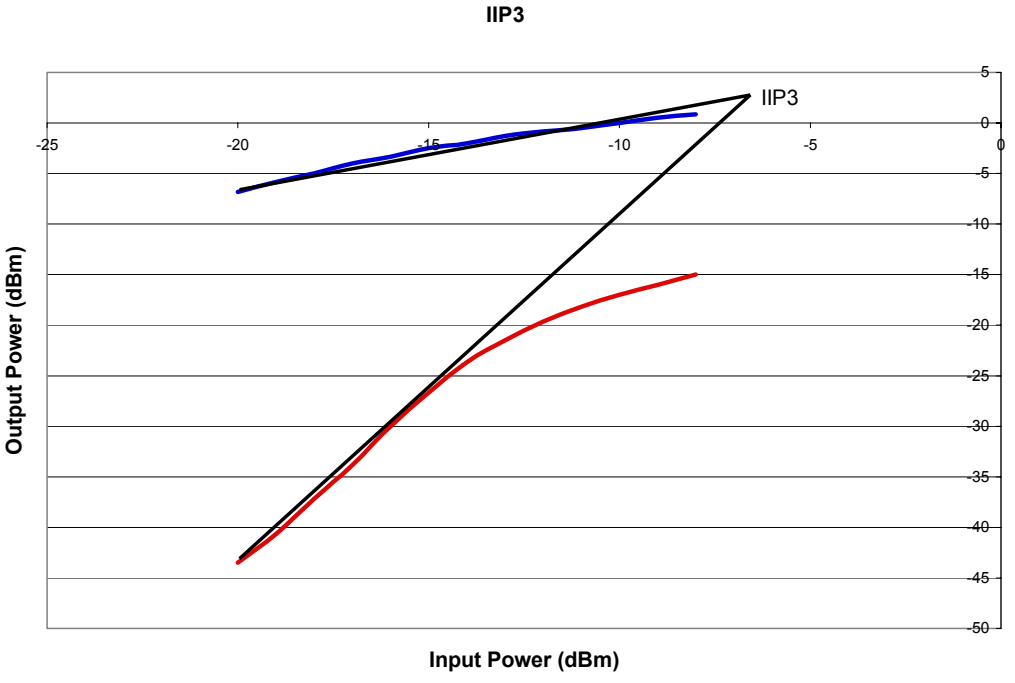



Figure 6.15: LNA Noise Figure, In- Phase (NF21) and Differential (NF31)

Also, as expected from a CMOS technology, the LNA doesn't achieve the high linearity of the SiGe version, due also to it's significantly higher gain. The LNA compression and intermodulation performance can be seen in Figure 6.16 to be -12 dBm (IP1dB) and – 7 dBm (IIP3). A die photo of the LNA can be seen in Figure 6.17, with a summary of its performance in Table 6.3.




(a)




(b)

Figure 6.16: LNA Input Referred (a) 1dB Compression Point and (b) IIP3

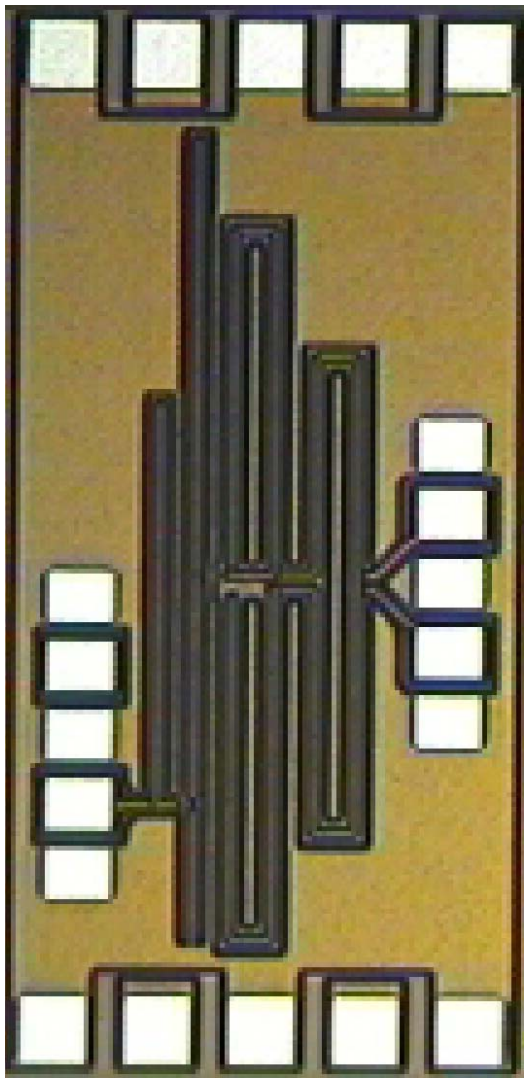



Figure 6.17: LNA Die Photo

Table 6.3: Summary of 24 GHz LNA Performance

| | | | |
|---|---|---|---|
| Frequency | 24 GHz | NF2 | 7.2 dB |
| S21 | 16 dB | NF3 | 10 dB |
| S31 | 6 dB | P1dB | -12 dBm |
| S11 | -14 dB | IIP3 | -7 dBm |
| S22 | -6 dB | Supply | 1.7V |
| S33 | -14 dB | DC Current | 11 mA |
| Phase Delta | 180° | | |

## 6.3 A 94 GHz SiGe LNA

A final LNA was designed for operation within the 94 GHz unlicensed communications band, once again employing a SiGe technology. Unlike the previous SiGe LNA design here the most advanced SiGe technology is employed, enabling amplifier design at frequencies far beyond any previous silicon circuits [41,42,43]. This considered, most of the advances in modern silicon technologies concern minimum feature size and transistor speed, but neglect the other challenges of the silicon platform like back end design and isolation [44,45,46]. These challenges are magnified in amplifier design (as opposed to VCO design) due to the additional design criteria which much be simultaneously met, which adds design complexity and makes the design more sensitive to process variations and modeling uncertainties.

The LNA described here is a single stage, single-ended design, demonstrating exceptional gain up to 110 GHz (test limitation). Due to measurement limitations, only

small signal s-parameters could be measured, with gain of up to 12.5 dB (at 94 GHz). Beyond being the fastest silicon amplifier to date, this gain (and the gain-BW product) would be considered exceptionally high for amplifiers at half it's operating frequency.

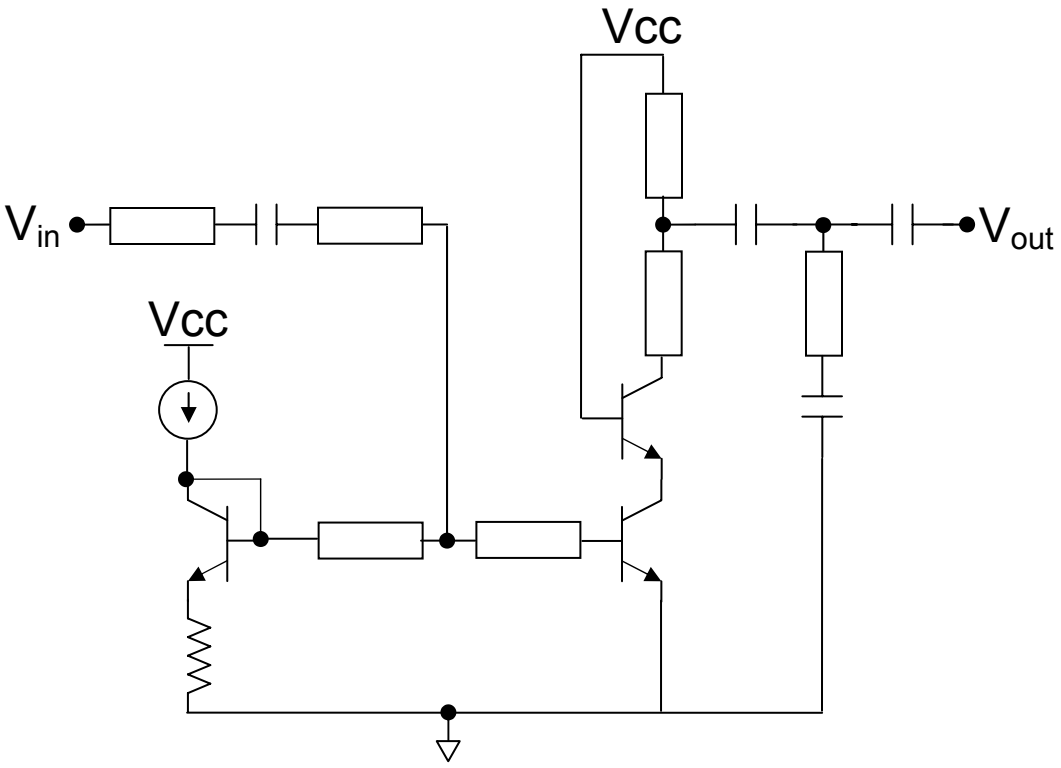



Figure 6.18: 94 GHz LNA Simplified Schematic

### 6.3.1 LNA Design

The 94 GHz LNA uses a simple cascode design, with series-shunt output matching, but no inductive degeneration, as can be seen in Figure 6.18. Early stages in the design flow incorporated a small degeneration transmission line, however the high base resistance of the HBT and parasitic wiring inductance through layout were enough to alleviate this need. Also, at high frequencies the effective inductance of the emitter of the cascode can introduce some real component through the miller

capacitance, improving the input match of the LNA (at the cost of gain and bandwidth). A variable bias source similar to that employed in the LNA described in section 5.2 was employed, chosen largely for its minimal noise contributions.

To achieve operation at these frequencies the transistors needed to be biased very near to maximum $f_t$, increasing the minimum possible noise figure for the LNA. While this high current increases the amount of shot noise contributed to the system, the devices were broken into a multiplicity of two devices to lower the base resistance, as well as ensure more uniform current distribution.

To increase the frequency of the output pole the cascode device was scaled smaller than the common-emitter input stage, allowing the same output current swing with a lower node capacitance (while staying beneath saturation of the transistor). Despite this, series-shunt matching was still required to achieve significant gain at these frequencies, and the high output impedance of the collector of the cascode was necessary to quell the miller effects of the two devices. Due to the low capacitance density available to decouple DC bias nodes, the base contact of the cascode device is capable of sustaining some AC components. Feedback through the miller capacitance could therefore incur oscillations if to large. Also, the high frequency of the amplifier allows there to be some feedback through the cascode into the miller capacitance of the common emitter stage, lowering of the input pole of the LNA.

### 6.3.2 Layout Considerations

In implementing the LNA the layout becomes the most crucial step, and is the driving force behind much of the electrical design. Beyond the hurdles of designing at a scale where the wavelength is comparable to the size of the IC, here added concern is required because the individual components (HBTs, Caps, etc) are of significant electrical length. Also, the incredible high frequencies make unmodeled wiring an

even greater concern, as does the effect of process variations on LNA matching. Considering that at higher frequencies the capacitance of a particular device (particularly the capacitance seen at the output of the LNA) becomes a significant part of the resonant match, minor variations across process corners or even during operation as created by variations in current density can impact the circuits matching. To address these concerns active area must be minimized, both to limit the effect of the device capacitance on the resonant matching networks, and to minimize the amount of wiring necessary for these devices. A blow-up of the active area of the LNA can be seen in Figure 5.19, occupying less than 30 μm x 30 μm.

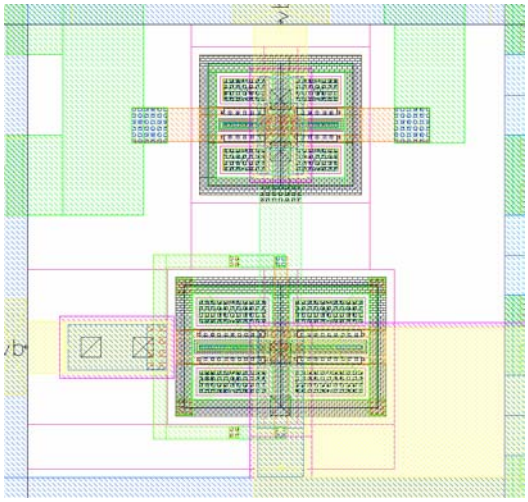


Figure 6.19: 94 GHz LNA Active Area

In Figure 6.19 the common-emitter and cascode stage can be seen at the bottom and top of the layout, respectively. In this layout the minimum possible size isn't determined by any electrical constraints, but rather physical design rules dictating the densities of deep trench isolation (due to planarization constraints). To combat this

constraint DT boundaries are shared where possible, evident by the intersections of the multiplicitied devices of the common-emitter and cascode stages.

Beyond the active areas (there are additional active devices for bias control, however they needn't meet the same stringent requirements as the carry only DC currents) the entire IC is constructed of carefully crafted transmission lines, capacitors, and pads. Many of the components necessary to assemble the back end (besides the active areas, only the top three metal layers are used) needed to be custom designed, including a small aspect ratio pad to optimize for electrical transparency. At these exceptionally high frequencies the pad capacitance is a major contributor to the resonant matching network, and it's electrical transparency is most important at the output port of the LNA, since within an actually system implementation that pad would need to be removed with minimal impact on the output match. Where possible transmission line junction design was performed within the cadence environment using the pre-existing layers for transmission line description. Pad design was performed using HFSS full wave simulator, a close up of the simulation structure can be seen in Figure 6.20, with its simulation results in Figure 6.21.

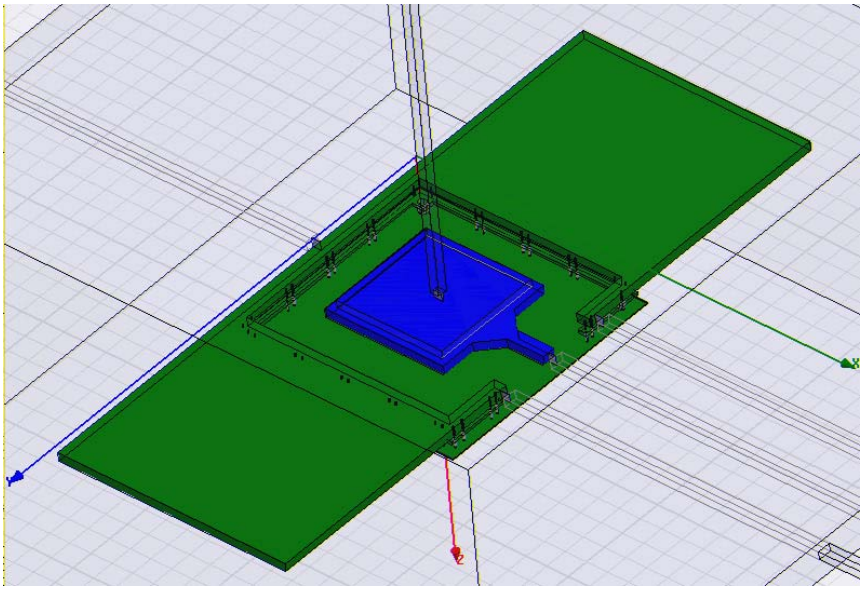


Figure 6.20: 94 GHz Pad Designed with HFSS

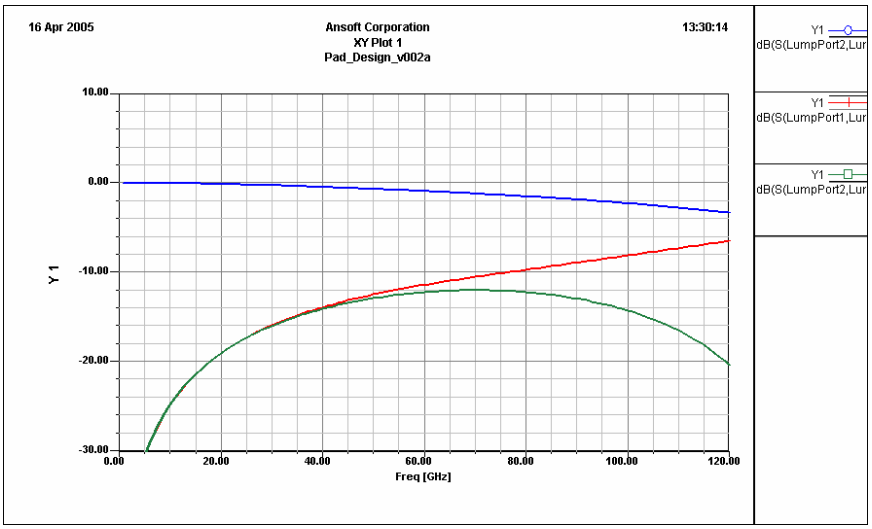



Figure 6.21: Simulation results for HFSS Designed Pad

Despite minimizing the area of the pad, another important design criterion was to use a metal back plane continuous with the back plane of the transmission lines. By using a metal back plane (rather than bare substrate) losses due to return currents flowing through the highly resistive silicon are mitigated, as they are instead restricted

to the conducting backplane. To satisfy these criteria the backplane of the pad must be thicker than the skin depth of the frequency at interest, which mandates the use of a higher metal layer. Using a higher metal layer also allows the pad backplane to be perfectly continuous with the backplane of the transmission lines (so chosen for reduced loss and improved DC power distribution), eliminating a reflective boundary.

As was discussed in previous sections, the relatively low capacitance density makes it difficult to create accurate AC grounds, especially in single-ended circuits. This is complicated by the condition that decoupling capacitors must be kept to a small size to avoid self resonance at high frequency, thereby lowering the effective silicon area available for decoupling. To combat this decoupling is placed as close as possible to the required nodes, with transmission lines terminating by wiring directly down (through vias) to heavily decoupled power planes beneath their backplane. Power and ground planes are interleaved to introduce additional background capacitance, and outside of the transmission line environment MIM capacitors are stacked above MOS type varactors to further increase the on chip capacitance.

### 6.3.3 Experimental Results

Due to the extremely high frequencies involved in this design testing was quite difficult, requiring collaboration with Cascade Microtech for small-signal measurements (the only yet available). These measurements can be seen in Figure 6.22.

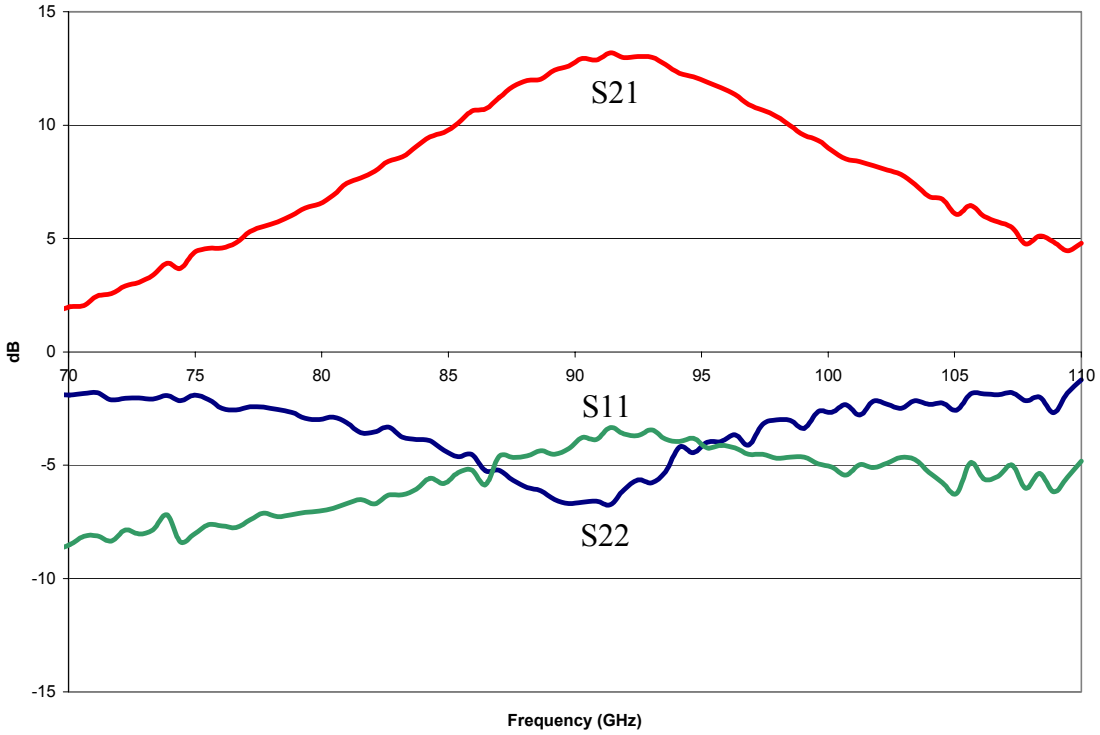



Figure 6.22: 94 GHz LNA Small Signal S-Parameters

From Figure 6.22 the small-signal gain can be observed to be almost identical to simulation (actually higher than simulation, which was at 12 dB), however with some degradation to the match (which were simulated to be -15 dB). This match can be attributed to the very low tolerance at the input/output nodes for variations in capacitances, which can be caused by device variation, parasitic deviation, and model inaccuracies. It is important to note these variations need only to be a few femto Farads to significantly alter the matching characteristics of the LNA.

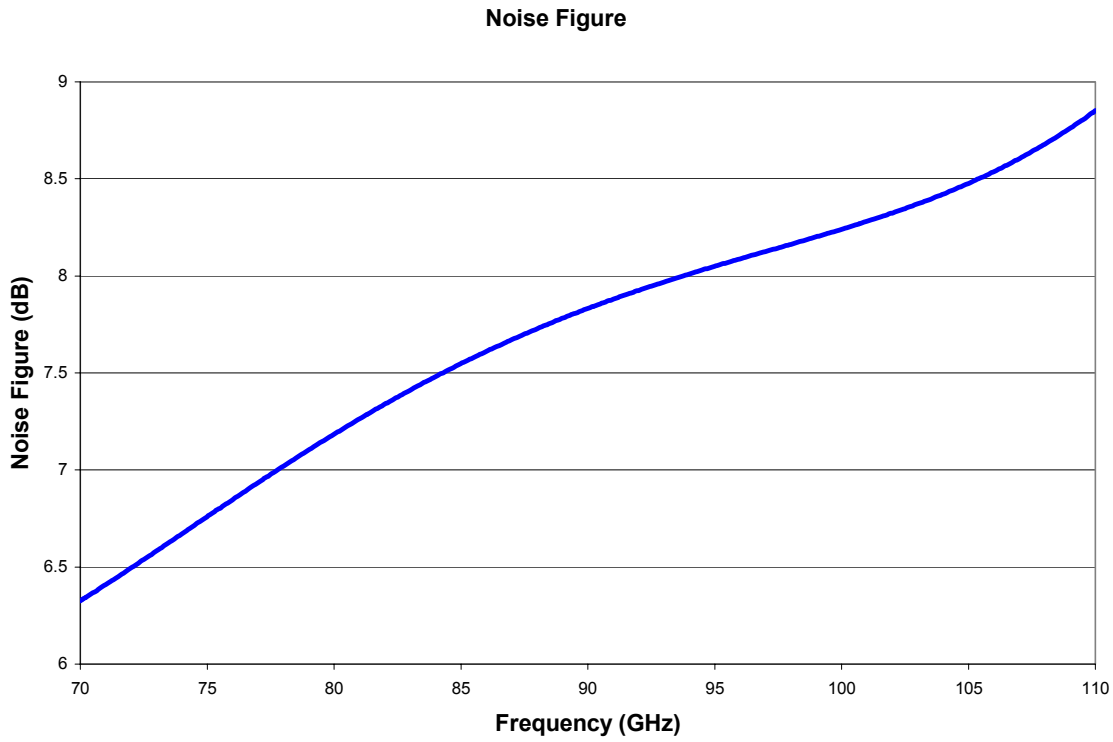



Figure 6.23: 94 GHz LNA Simulated Noise Figure

Due to the unavailability of a calibrated noise source at the frequency range in question, only simulated Noise Figure results are available. Figure 6.23 shows the simulated noise figure of the LNA, with a noise figure of 8 dB at 94 GHz. This high noise figure demonstrates the increased noise effects with higher frequency, and demonstrates one of the most prevalent challenges of mmWave transceiver design. Coupled with the increasing atmospheric attenuation at higher frequencies this further degrades the SNR of the received signal thereby limiting the range. This condition often dictates the design of other elements of the receiver, typically mandating higher gain before the mixer and baseband components.

While the high attenuation characteristics of the atmosphere at mmWave frequencies may seem to make receiver linearity less of a concern (due to the lower expected received power levels), this is offset somewhat by the need for high receiver gain to decrease the overall system noise figure. This criterion becomes exceptionally hard to design for due to the restrictions placed on device size by operating frequency and noise requirements. The linearity of the LNA can be seen by observing the 1dB compression point, as seen in Figure 6.24.

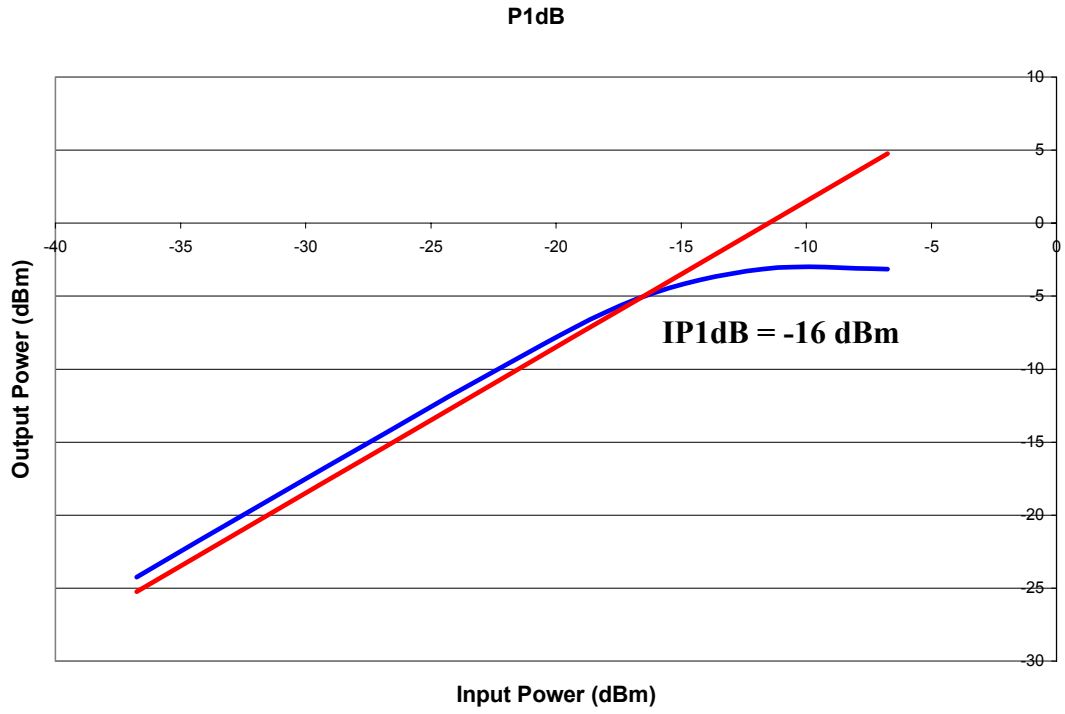



Figure 6.24: 94 GHz LNA Simulated Input Referred Compression Point (IP1dB)

In Figure 6.24 the IP1dB can be observed to be -16 dBm. While this may seem low, given the attenuation characteristics of the atmosphere at these frequencies (approaching 100 dB/Km), input power levels of this magnitude would be expected at ranges beyond a few meters. This is made more likely due to the lower available

output power at higher frequencies, at best in neighborhood of 20 dBm. In reality, it is the companion transmitter that may be a more pressing concern for receiver linearity, since isolation between the two becomes more difficult at higher frequencies. To achieve a reasonable useful range with the wireless link the receiver must be sensitive down to exceptionally low power levels, perhaps as low as -100 dBm. As such, assuming the most extreme case where the system is running in a full-duplex manner as much as 120 dB of isolation between the transmitter and receiver might be required. While this requirement can be mitigated by the fact that the case of the transmitter operating simultaneously and at the same frequency of the receiver is incredibly unlikely, it still demonstrates one of the greater difficulties in mmWave wireless design.

Notwithstanding the limitations in measurement abilities, this LNA is the fastest known silicon amplifier to date (discounting buffers employed on certain silicon VCO's, which have been demonstrated at higher frequencies). A summary of its performance can be seen in Table 6.4, a die photo of the LNA can be seen in Figure 6.25.

Table 6.4: Summary of 94 GHz LNA Performance

| | | | |
|---|---|---|---|
| Frequency | 94 GHz | NF | 8 dB |
| S21 | 12.5 dB | IP1dB | -16 dBm |
| S11 | -4 dB | Supply | 2.0 V |
| S22 | -7 dB | Current | 7.9 mA |

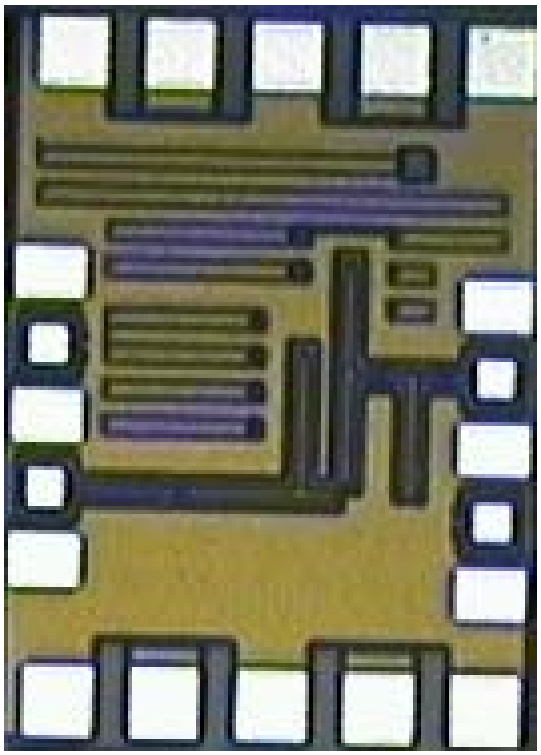


Figure 6.25: 94 GHz LNA Die Photo

## 6.4 Conclusions

In this chapter three LNAs are presented showing continued evolution in mmWave design beyond 100 GHz. Similar to the development of VCOs discussed in Chapter 4, here certain techniques were required to enable reliable operation at exceptionally high frequencies. Beyond an electrical design methodology eliminating non-critical elements, a careful physical design methodology was required to mitigate unwanted (and unmodeled) parasitics. Also, carefully implemented and in some instances novel matching networks were required to achieve reliable operation into the mmWave regime, most notable the use of series-shunt output matching to expand the bandwidth of the output pole. As is evident in the 24 GHz CMOS and 94 GHz SiGe LNAs these techniques are unified by the carrier (Silicon), and are not exclusive to a

particular type of device, as was forecast with the discussion of the BEOL limiting factors in chapter 2.

# Chapter 7 Wireline Design and Innovation

Once the techniques for mmWave operation were developed using wireless transceiver components, they were applied to more conventional wireline circuits to observe the bandwidth extension possibilities in digital applications. Among these circuits were mulitplexers, demultiplexers, DFFs (Flip-Flops), and static dividers. Through this examination it will be shown that certain techniques for bandwidth extension, that are applied with low $f_t$ technologies, are useful at mmWave frequencies, whereas other are not. While it is often that case that some of these techniques become unnecessary with faster devices, it is just as likely that the parasitics they introduce offset the benefits they hope to achieve.

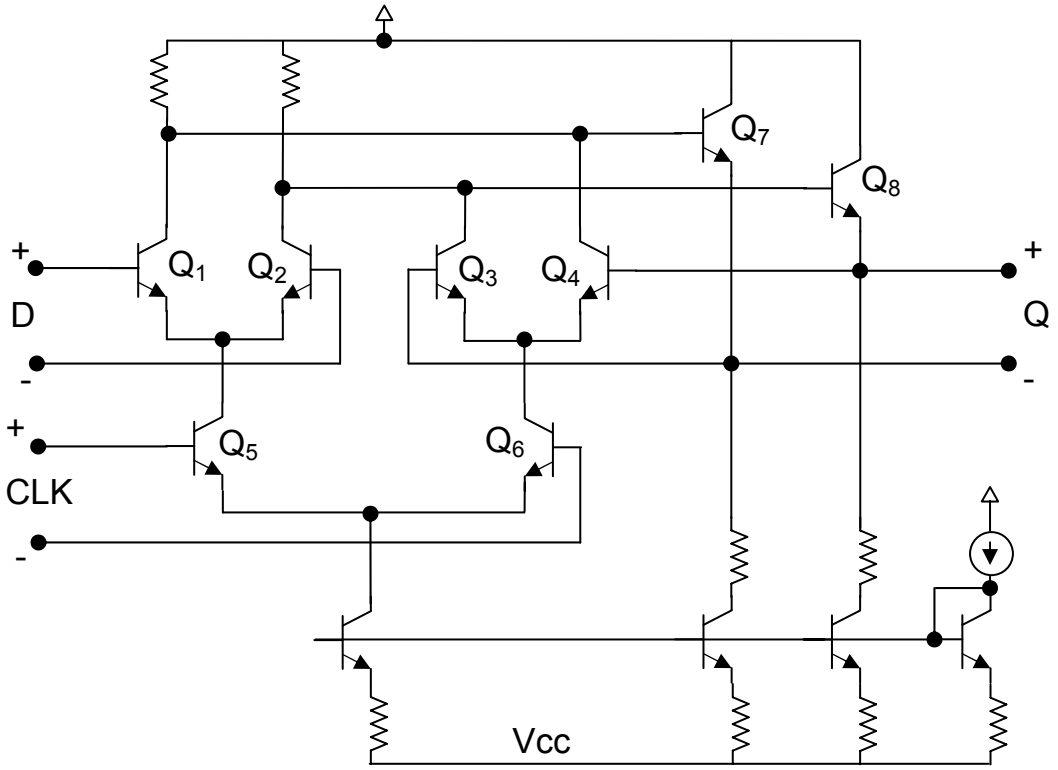



Figure 7.1: High Speed Latch Using Emitter-Coupled Logic

## 7.1 mmWave Latch Design

While there are various techniques for implementing a latch, high frequency latch design typically relies on emitter-coupled logic to achieve optimum speed. A basic emitter-coupled logic latch can be seen in Figure 7.1 [47]. By using stacked differential pairs the circuit can operate at exceptionally high frequencies by avoiding saturation of the devices. As such the voltage swing across any of the devices is well beneath rail-to-rail swings in conventional (CMOS) latch operations, often around a few hundred millivolts. This latch operates by using transistors $Q_5$ and $Q_6$ to steer current (based on the clock input) into the two differential pairs formed by $Q_1$-$Q_2$ and $Q_3$-$Q_4$. The pair $Q_1$-$Q_2$ received the input from the prior stage (another latch in the case of a flip-flop), while the pair $Q_3$-$Q_4$ hold the data from the previous input. Emitter followers $Q_7$ and $Q_8$ are used to level shift the outputs and feed them back into the hold pair of transistors.

The limiting factors in this circuit then become how fast the clock pair $Q_5$-$Q_6$ is able to switch the current between the two circuits (which typically depends largely on how fast the clock switches), and how quickly the collector voltages of the write and hold pairs are able to switch. While the former concern is largely address in the clocking network, the later is a concern only of the latch. Since the collector of the write and read pair sum currents together across the load resistors it is a voltage mode node (unlike the collectors of the current steering pair which operate mostly in current mode), making it largely susceptible to capacitive loading. Any capacitances on the node will restrict the bandwidth by lowering the output pole of the transistors, an effect similar to those described in the discussions of wireless circuits. This considered most of the techniques for bandwidth extension deal with increasing the bandwidth at this node.

### 7.1.1 Inductive Peaking

Perhaps the most apparent technique for extending the bandwidth of the latch, at least from the perspective of the techniques used for improved wireless performance, is inductive peaking of the load resistors to resonate out the capacitance at the collectors. An example of this circuit is that shown in Figure 7.2 [12].

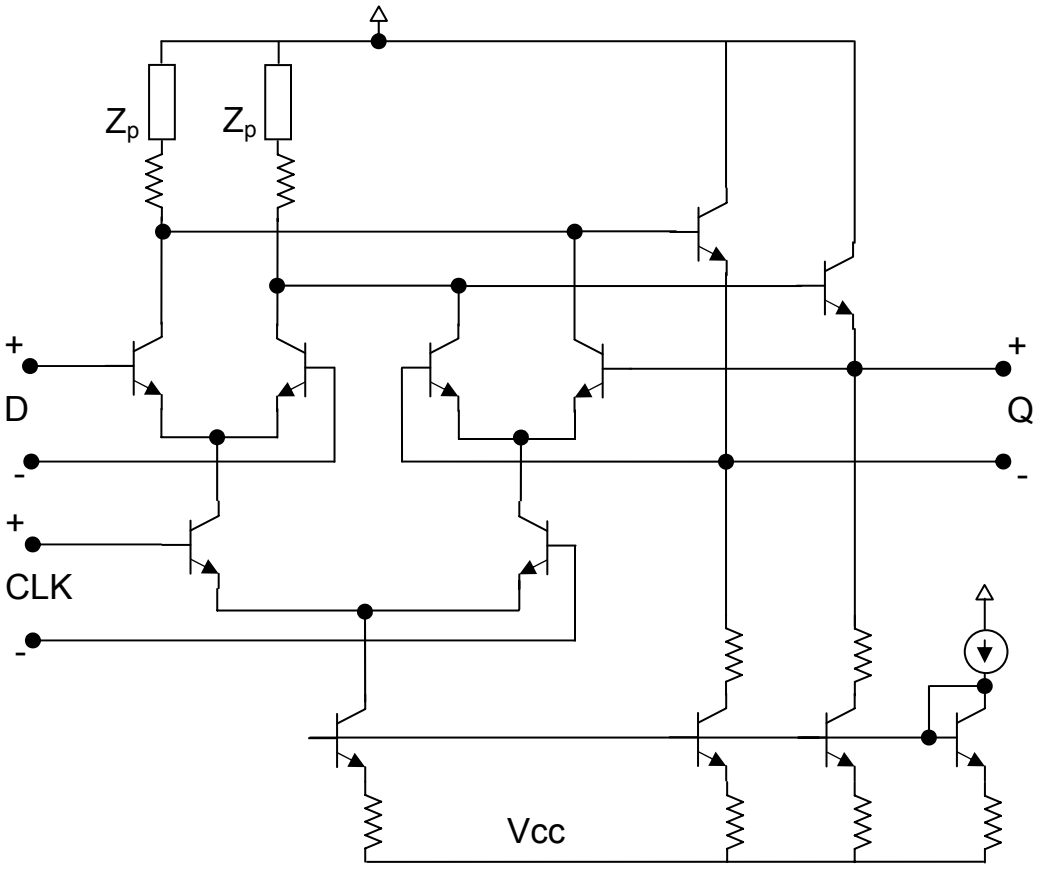



Figure 7.2: High Speed Latch with Inductive Peaking

There are, however, certain drawbacks to the circuit in Figure 7.2. Foremost, since there is some feedback through the hold pair stability is a concern, as the inductive peaking will introduce some resonance. More of a concern, however, is the

increased area the latch must occupy to include inductive peaking. This isn't typically a concern in wireless systems because few instances of peaking are required, however in a digital system many of these latches may be tiled together, such as in a MUX or DeMUX. If the latch size is increased substantially through inductive peaking excess wiring is required to connect them, thereby introducing new parasitics and offsetting the benefits of the peaking (and potentially making the system worse than if no peaking was employed). Also, this peaking is typically employed on the top metal layers, thereby limiting the abilities to thoroughly route power, which can be a large detriment considering the substantial powers consumed in large scale digital circuits.

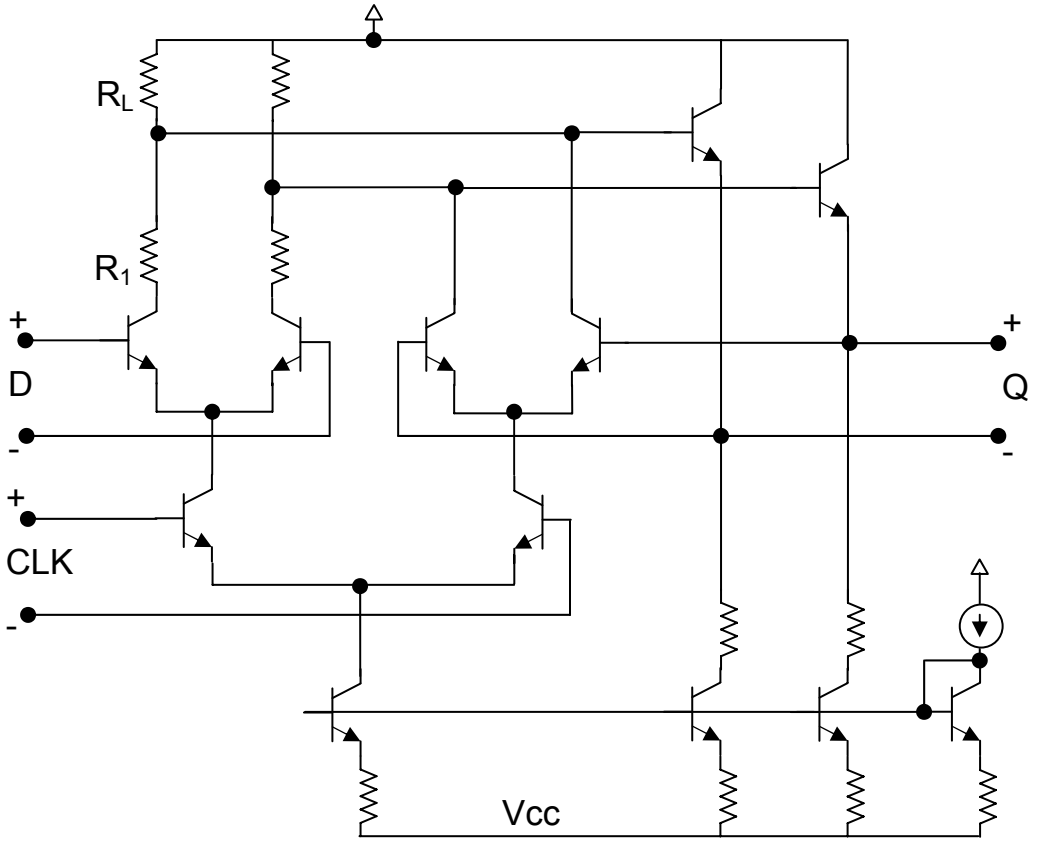



Figure 7.3: High Speed Latch with Split Resistive Loads

### 7.1.2 Split Resistive Loads

Another technique commonly used for improving the bandwidth of a latch is to introduce another resistor into the collector path of the write pair of transistors, reducing the gain of that pair [48,49]. This circuit can be seen in Figure 7.3. By doing so the gain of the write pair of the latch is decreased, allowing for faster transitions. In this circuit configuration the output voltage level of the write pair is lowered to:

$$V_c = \frac{R_L}{R_1 + R_L} V_L \tag{7.3.1}$$

Compared to inductive peaking, however, this technique introduces marginal improvements over the conventional latch, and at the cost of increased area of the latch. Introducing these two resistors not only increases the amount of wiring required to route amongst multiple latches, but also introduces further parasitics through the additional resistor. With these restrictions in mind, this technique is not particularly useful for mmWave latch design.

### 7.1.3 Asymmetric Latch

In an asymmetric latch the hold pair of transistors ($Q_3$ & $Q_4$ in Figure 7.1) is reduced in size relative to the write pair ($Q_1$ & $Q_2$). In doing so the parasitic capacitance at the resistive load is decreased, extending the bandwidth of the latch. This technique is possible because the purpose of the hold pair is to simply maintain the value previously written across the resistive loads (whereas the write pair has to change the voltage), so the pair does not need as much gain.

There are certain risks to this technique, however it is still the best suited to mmWave operation. Since the two devices composing the clock pair are the same size, the hold pair of transistors cannot be made to much smaller out of risk of saturating the devices. In reality, since high frequency operation will require the write pair to be biased near $f_t$, the hold pair will be biased above $f_t$, diminishing their effect. This increased current density will give the hold pair a greater collector capacitance than it otherwise would, although it will still be less than that of a larger device. The largest benefit to this technique is that is introduces no new elements to the latch, and therefore doesn't increase the amount of wiring necessary in a system composed of multiple latches.

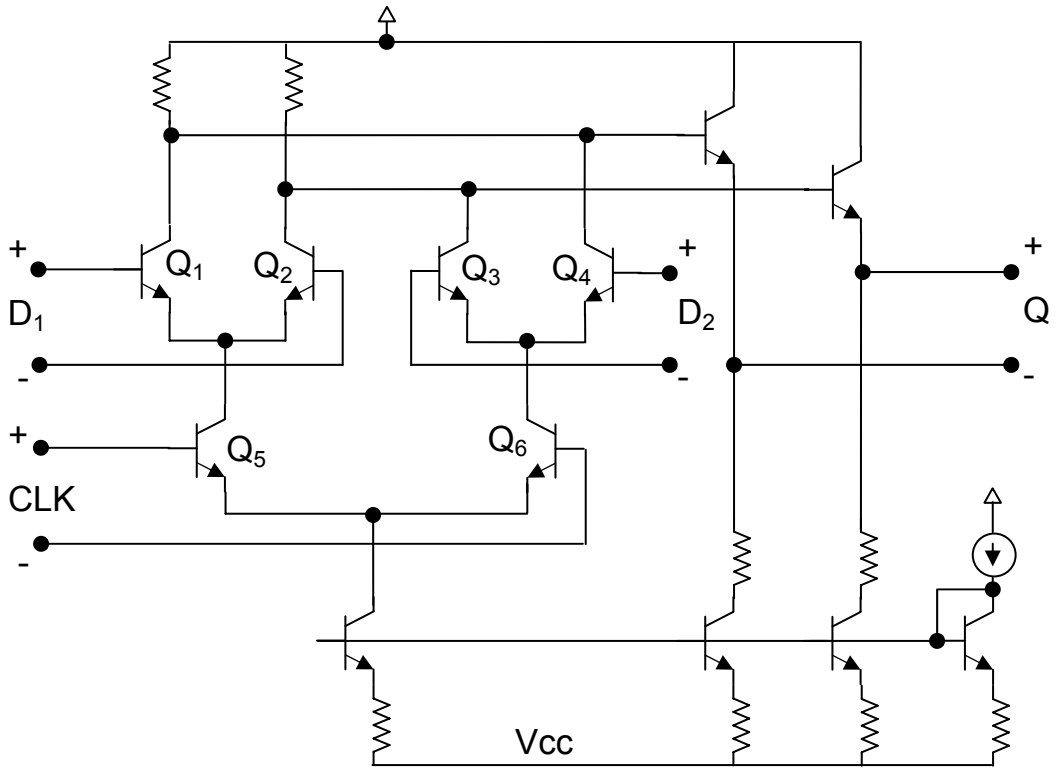



Figure 7.4: High Speed Selector using Emitter-Coupled Logic

## 7.2 mmWave Selector Design

An ECL selector is very similar to an ECL latch, as they are both based off of an ECL gate. Seen in Figure 7.4, this circuit also uses a differential clock input to steer current between two differential pairs, whose output currents are combined across shared loads. Unlike the latch described in section 7.1, here both of the differential pairs ($Q_1$-$Q_2$ & $Q_3$-$Q_4$) receive an input signal, and the output of the selector is chosen by the clock signal. In this way, a selector is a simple multiplexer.

Since there is no disparity between the functions of the two differential pairs, the only bandwidth extension technique that can be applied is inductive peaking. While there are still the drawbacks to inductive peaking as described in the previous section, since there are typically very few selectors in a given circuit, inductive peaking can be employed more readily without a huge cost of increased wiring.

## 7.3 High Speed Buffers

Within a high speed digital application broadband buffering is often one of the most crucial, and difficult, challenges to overcome. While the upper bandwidths on the system may rate into the hundreds of gigabits per second the slowest rates may be in the megabit per second range, requiring tremendously broadband amplification. This, or course, may be impossible in most conventional amplifiers due to their frequency response, which we have already noted can be dire given the high parasitic behaviors at increasing frequencies. With this in mind, certain topologies must be employed to assure operation over the entire intended bandwidth of the buffer.

### 7.3.1 Emitter Followers

The simplest commonly used amplifier in digital applications is the emitter follower (common-collector), as shown in Figure 7.5 [50]. While it is an exceptionally

simple circuit, it is invaluable to ECL design due both to its high frequency operation and level shifting capabilities.

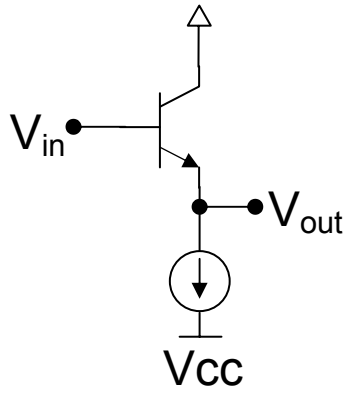



Figure 7.5: Emitter Follower

One benefit to the emitter follower, as can be seen in Figure 7.1, is its high input impedance and low output impedance. Therefore in its function to buffer and level shift the outputs of ECL gates it doesn't significantly load the collector nodes of the differential pairs. Also, an emitter follower is a largely linear amplifier with little voltage gain and mostly current gain. Since the voltage swing at the emitter of the device is near to that at the base there is no capacitance multiplication effect (and, since the collector is tied to an AC ground there is no miller effect), so the input pole is at a relatively high frequency.

### 7.3.2 Emitter Coupled Pair

Another frequently used buffer for digital applications if the emitter coupled pair [51]. The emitter coupled pair is created by coupling a pair of common emitter amplifiers at their emitters, typically over an active current source. A simplifier version of the emitter coupled pair can be seen in Figure 7.6(a).

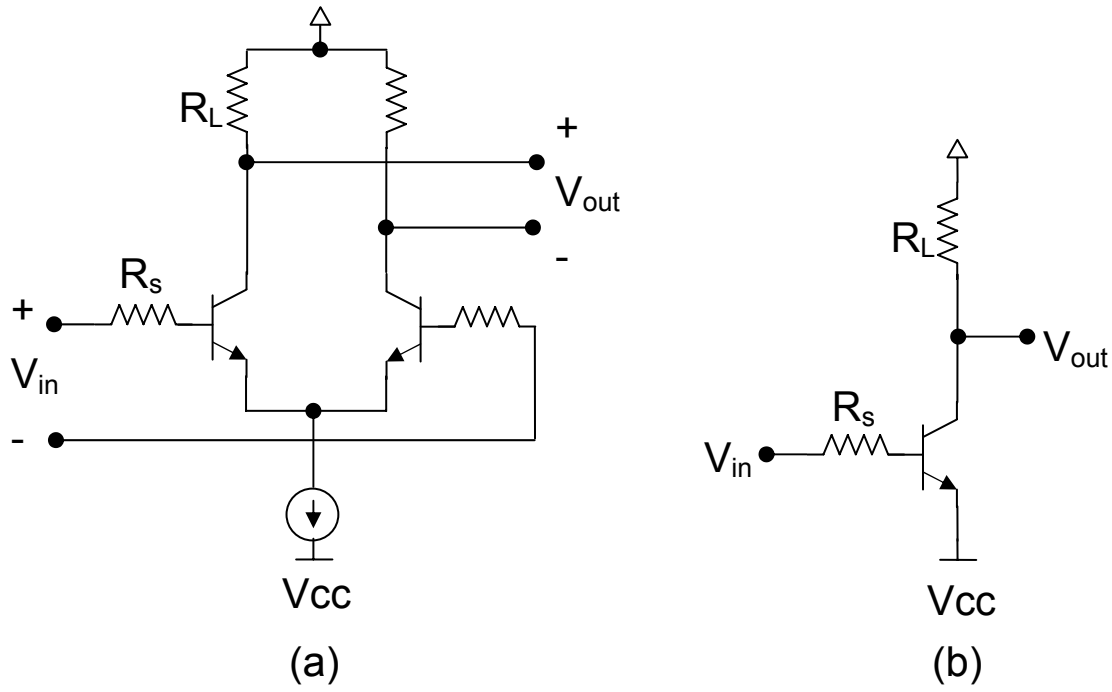



Figure 7.6: (a) Emitter Coupled Pair and (b) Half Equivalent Circuit

The half differential shown in Figure 7.6(b) circuit behaves similar to the LNA configurations described in chapter 4. In this circuit there are two capacitances that will create a dominant input pole, those being the base-emitter capacitance ($C_\pi$) and base-collector capacitance ($C_\mu$). That pole can be found at the frequency [52]:

$$\omega_p = \frac{1}{\left[R_s \| r_\pi\right]\left[C_\pi + C_\mu\left(1 + g_m R_L\right)\right]} \tag{7.3.1}$$

In equation 7.3.1 the miller multiplication effect can be seen in the term $1+ g_mR_L$, which can be mitigated through cascoding of the device (this, however, is often not possible with the headroom constraints of digital systems). Note, also, that the

input resistance $R_s$ needs to be minimized to keep from increasing the pole frequency substantially, as the product of $R_s$ with $r_\pi$ is dominated by the source resistance.

While this configuration is typically not tremendously broadband, it is often necessary within a digital system, especially within the output stages of a wired transmitter. The differential amplifier can deliver a large voltage swing across a 50 Ω load (to ground), which makes it a very attractive configuration for the final stage of buffering in most wired links. While in its most basic incarnation it has restricted bandwidth, certain techniques can be applied to increase its bandwidth.

### 7.3.2.1 Emitter Degeneration

One technique for expanding the bandwidth of an emitter coupled pair is through emitter degeneration, of either the purely resistive type or using a parallel RC network [52]. An example of these two types of circuits can be seen in Figure 7.7.

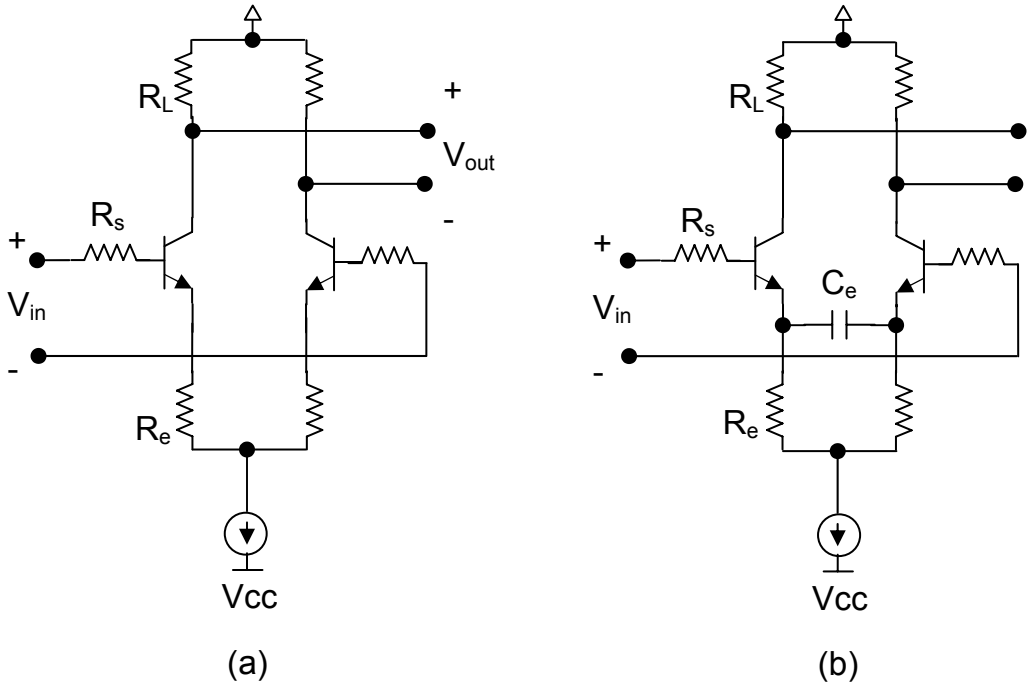



Figure 7.7: (a) Resistive Degenerate Emitter Coupled Pair and (b) RC Degenerated Emitter Coupled Pair

In Figure 7.7(a) resistive degeneration is shown. Pure resistive degeneration functions by decreasing the low frequency gain, essentially normalizing it to the gain at some higher frequency level. An example of the frequency response of this amplifier can be seen in Figure 7.8.

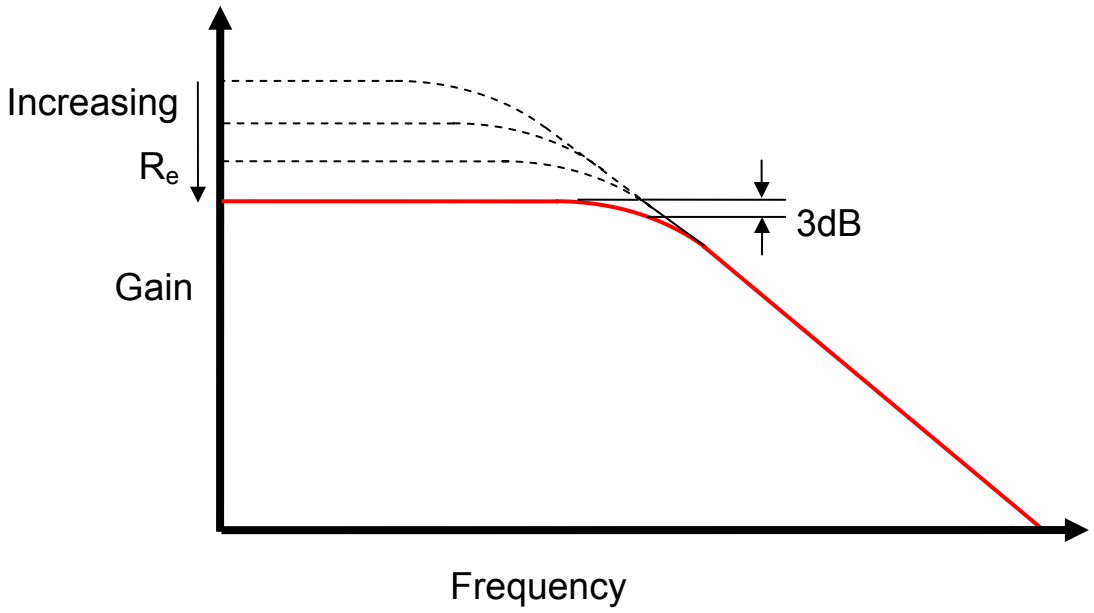



Figure 7.8: Effect of Resistive Degeneration on an Emitter Coupled Pair

In Figure 7.8 it can be seen that by increasing the degeneration resistance the low frequency gain is decreased, however the bandwidth is increased. One drawback of using purely resistive degeneration, however, is the 3dB rolloff at the cutoff frequency. This rolloff is typically compensated by introducing capacitance to the degeneration network, as shown in Figure 7.7(b). The capacitor effectively bypasses the resistance at higher frequencies lowering the impedance to the coupled node, thereby introducing a pole to the system. The transfer function of the RC degenerated half equivalent circuit can be written as:

$$\frac{I_c}{V_{in}} = \frac{g_m\left(2R_eC_es+1\right)}{2R_sC_\pi R_eC_es^2+\left(R_sC_\pi+R_eC_\pi\right)s+R_e/r_\pi+R_s/r_\pi+R_eg_m} \tag{7.3.2}$$

From equation 6.3.2 the solution for pure resistive degeneration can be extracted by setting $C_e = 0$. In doing so it is observed that the pole created by the capacitive degeneration (at $1/2R_eC_e$) drops away, removing the gain boosting effect of capacitive degeneration.

Despite these advantages, there are certain drawbacks to using emitter degeneration. Degeneration resistance will introduce new thermal noise contributors to the circuit, which could contribute to ISI and jitter within the system. Also, the large size of the resistors and, more importantly, the capacitors can introduce significant parasitics to the circuit by requiring additional wiring. As such, while it isn't without application in mmWave wireline design, these techniques are not applied in the design examples which will be described in chapter 8.

#### 7.3.2.2 Inductive Peaking

Another bandwidth extension technique, which was previously described in the context of the latch and selector design, is using shunt inductive peaking in series with the load resistors to resonate with any output capacitance. As has been previously discussed, inductive peaking can be employed to introduce a zero to compensate the output pole of the buffer. A simple emitter coupled pair using inductive peaking at the output can be seen in Figure 7.9.

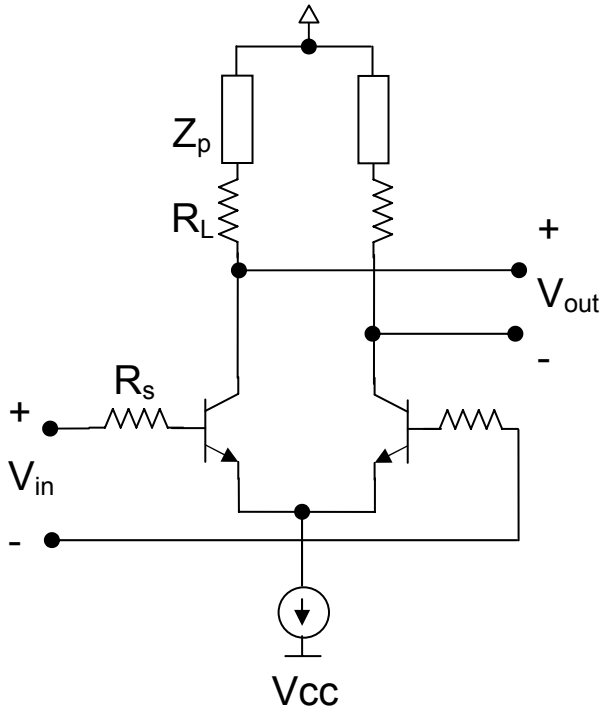



Figure 7.9: Emitter Coupled Pair with Inductive Peaking

Unlike in the case of the inductively peaked latches and selectors, this circuit is quite useful in mmWave digital design. Since it is typically restricted to the output of the system, the prior complication of the introduction of unwanted wiring is mitigated. Also, beyond extending the gain bandwidth of the amplifier the inductive peaking can help the output matching at higher frequencies as well, resonating out some of the effects of the pad/package parasitics.

### 7.3.3 Cherry Hooper Amplifier

The final extended bandwidth buffer which will be discussed here is also one of the most frequently used amplifiers in high speed digital applications. Often the

mainstay of the clocking of these systems, the Cherry Hooper amplifier is characterized by an incredibly broadband response, typically much greater than the proceeding amplifier topologies (save for the emitter followers). A simplified schematic of a Cherry Hooper amplifier can be seen in Figure 7.10 [53]:

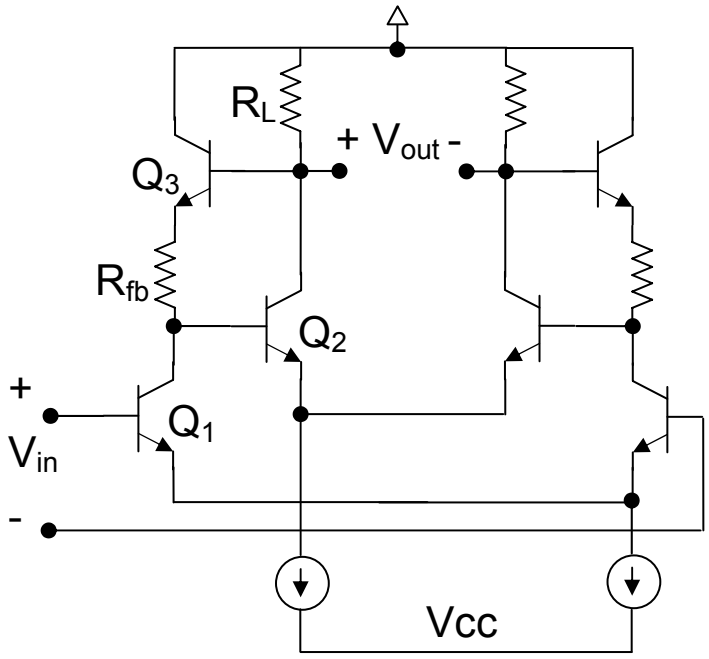



Figure 7.10: Cherry Hooper Amplifier with Emitter Follower Feedback

In the Cherry Hooper the feedback loop through $Q_3$ and $R_{fb}$ serve two purposes, to broaden the response of the output stage ($Q_2$) and lower the load resistance of the input stage ($Q_1$). By lowering the load resistance seen by device $Q_1$ the input stage operates largely in current mode, mitigating the effects of the miller capacitance of this device. This effect can easily be recognized by deriving a simple expression for the input impedance of the second stage (the load impedance of the first stage) to be:

$$R_{in} = \frac{R_{fb}}{g_m R_L + 1} \tag{7.3.3}$$

Which approaches $1/g_m$ as the feedback resistance approaches the load resistance. This load resistance is typically much smaller than a comparable load resistance, reducing the miller effect of the first stage to:

$$C_{eff} = C_{\mu}\left(1 + g_{m1} / g_{m2}\right) \tag{7.3.4}$$

Assuming that the two stages have equal $g_m$, the Miller multiplication is simply a factor of two.

Similarly, the feedback loop around the second stage increase the bandwidth of the amplifier by returning a current proportional to the output voltage to the base of the device $Q_2$. Since the output impedance of the emitter follower in the feedback loop is much less than that of the feedback resistance ($1/g_m$ vs. $R_{fb}$) a simplified closed loop transfer function can be written for the second stage as [12]:

$$\frac{V_{out}}{I_{A1}} = \frac{R_{fb}{}^2 C_{c1} C_{\mu 2} s^2 + \left(g_{m2} R_{fb} C_{\mu 2} + C_{c1} - C_{\mu 2}\right) R_{fb} s + g_{m2} R_{fb} - 1}{R_{fb}\left(C_{c1} C_{c2} + C_{\mu 2} C_{c2} + C_{\mu 2} C_{c1}\right) s^2 + \left(C_{c2} + g_{m2} R_{fb} C_{\mu 2} + C_{c1}\right) s + g_{m2}} \tag{7.3.5}$$

Where $C_{c1}$ and $C_{c2}$ represent the capacitances seen at the collectors of transistors $Q_1$ and $Q_2$, respectively. Here the pole frequency is expanded to $\sim 2g_{m2}/(C_{c1}+C_{c2})$, which is much greater than that for a typical common-emitter stage ($1/R_L C_{c2}$).

## 7.4 mmWave Wireline System Design

Using only the afore mentioned components a multitude of digital communications circuits can be created, including high speed multiplexers, demultiplexers, static dividers, and flip-flops. These circuits are the most commonly used for high data rate communications, and are typically the fastest circuits in a digital system. Despite the advantages of the subcircuits already discussed, there are still many challenges in system development. As was mentioned throughout the previous sections, certain design techniques that have the ability to increase the bandwidths of individual sub circuits are ill equipped for high frequency design due to the compromises they require at a system level. It is in these compromises that the difference between a system that operates at a high speed relative to the abilities of the devices, vs. those that run at a high speed relative to the intrinsic capabilities of silicon, are revealed. This further underscores that the limitations of mmWave design are not fundamentally linked to the limitations of the transistors, but rather the peripheral elements in a silicon environment.

### 7.4.1 mmWave Multiplexer Design

While many topologies exist for multiplexer design, the most commonly used topology for high frequency systems is the tree structure employing five latches and a selector, as can be seen in Figure 7.11 [54].

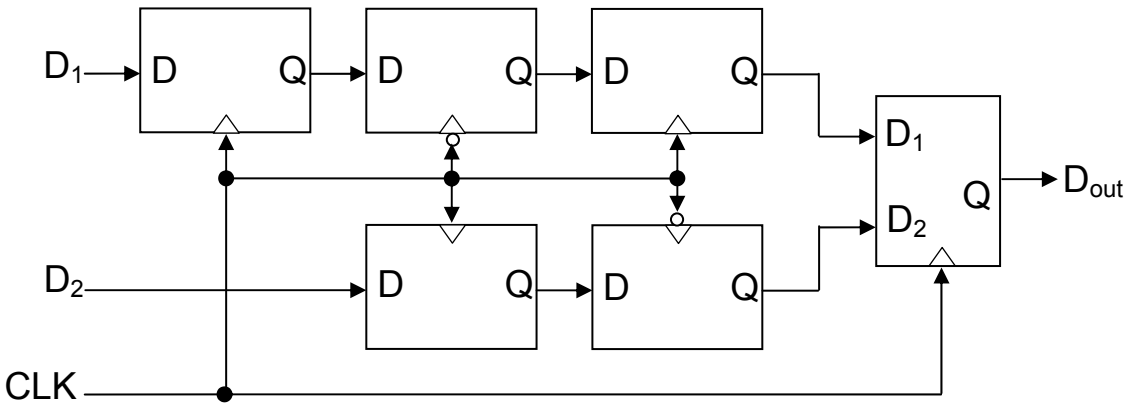



Figure 7.11: 2 to 1 MUX Using a Tree Architecture

In Figure 7.11 a 2 to 1 MUX can be seen, however high order MUXs can be created by connecting several of these together. Note that there is no retimining of the output in this configuration, making it a half rate design (the clock runs at half the maximum data rate). By doing so the circuit is able to operate at twice the highest frequency at which its subcircuits can be driven, doubling the MUXs maximum data rate.

In this MUX the clock distribution is shown as being a simple input, however this is one of the most challenging parts of design of any digital system. For proper operation, the clock phase seen at any of the subcircuits must be in proper phase alignment with the other circuits (or 180º out of phase for the inverted inputs), otherwise the circuit will suffer from increased ISI, Jitter, and may not operate at all. As will be examined in the next chapter, doing so often requires carefully floorplaning of the subcircuits employed, parallel clock buffers to reduce the fanout of any one buffer and allow for improved high frequency operation, and phase matched wiring at every interconnect to ensure minimal clock skew.

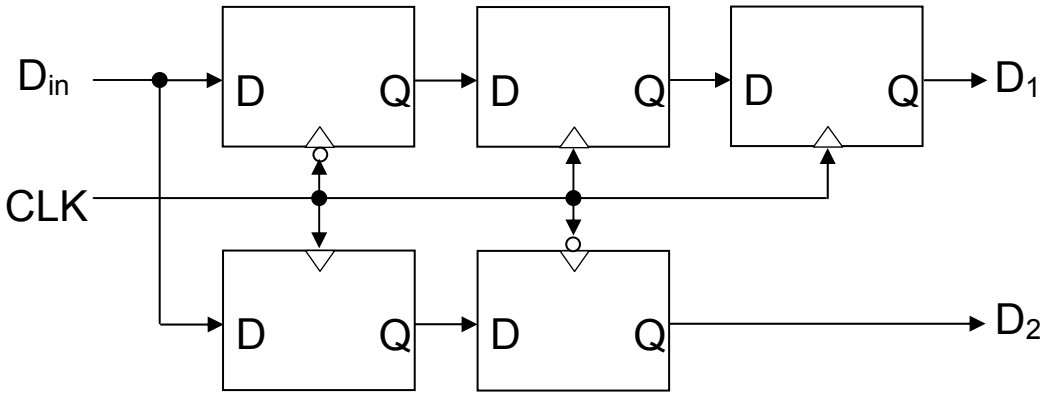



Figure 7.12: 1 to 2 DeMUX Using a Tree Architecture

### 7.4.2 mmWave Demultiplexer Design

Complimentary to the tree type MUX described in the preceding section, a DeMUX can be created using only the components described within this chapter. Simpler in design than the MUX, the DeMUX has no selector and instead divides the received signal and feeds it two parallel branches of latches, as shown in Figure 7.12 [50]. The clock then writes the input alternately into the first two latches, reconstructing the data that was previously combined through a MUX. As with the MUX design, the highest frequency DeMUXs typically use half rate system design to relax the requirements on the subcircuits employed. Also, here again the stringent requirements for clock buffering and distribution apply, mandating a lot of the subcircuit design compromises described earlier in the chapter.

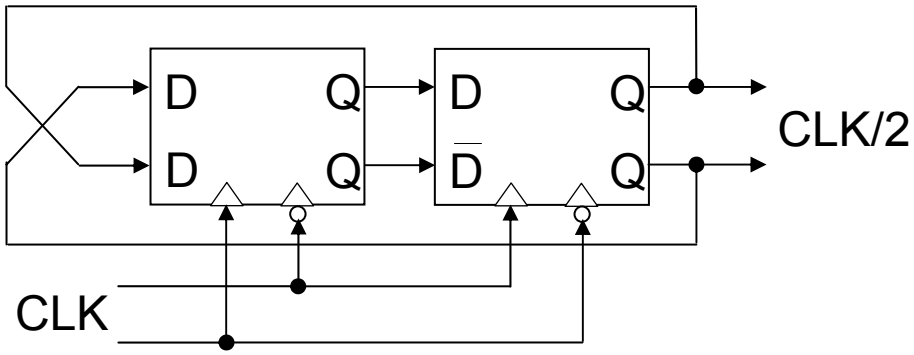



Figure 7.13: Static Divider using Differential Latches

### 7.4.3 DFF and Divider Design

The latches described above can also be assembled in pairs to create either a D flip-flop or a static divider. In the flip-flop two latches are combined in series to allow the data to be held between them, and it can be seen in both the MUX and DeMUX. A static divider is similar to this circuit, only with the outputs off the flip-flop cross coupled back into the inputs. In this configuration the circuit can be used to divide the clock signal by two (and can also be used to divide a differential signal into a quadrature signal). The flip-flop, aside from being used for signal alignment and selection within the MUX and DeMUX, can also be used to retime the outputs/inputs of the MUX/DeMUX. The divider, which can be seen in Figure 7.13 [49], is often used to divide the clock down to allow for multiple MUXs/DeMUXs to be connected together, with each successive branch (from the full rate input/output) needing a clock frequency at half the frequency of the prior stage. As such, in a system requiring clock division the divider often becomes the limiting factor on operation, since if the latches within the divider cannot switch at the rate of the clock some frequency other than the

desired CLK/2 will be created, destroying the operation of the other circuits (MUXs/DeMUXs).

# Chapter 8 Wireline Design Examples

Using the circuits described in chapter 7 several systems were designed for operation above 100 GB/s. These circuits include a 4 to 1 MUX, 1 to 4 DeMUX, 60+ GHz Divider, and 60+ GB/s DFF. These circuits were all realized using the same advanced SiGe technology as the fastest wireless circuits (BiCMOS8HP).

Certain changes to the subcircuits described above were performed to enable reliable operation in this technology. Due to the inductive behaviors of the outputs of the emitter followers differential loads were employed to damp any resonances. Also, to prevent instabilities due to peaking in the output buffers (of the MUX) the Q factor of the transmission lines employed were degraded by moving them to a lower metal layer (the second metal layer from the top). Also, as was mentioned previously parallel buffers with a low fanout (2 latches per buffer) were used for clock distribution, even in the quarter rate section of the MUXs/DeMUXs to ensure symmetry across the system.

## *8.1 4 to 1 MUX*

### 8.1.1 Design and Layout Considerations

The 4 to 1 MUX uses three 2 to 1 MUXs cascaded together, with separate clocks provided at half-rate and quarter-rate (since there is no full-rate retiming no full-rate clock is required). A schematic of the 2 to 1 MUX with parallel clock buffering can be seen in Figure 8.1 [55]. In Figure 8.1 it can be seen that Cherry-Hooper amplifiers are used for buffering the clock, due to their abilities to limit the sinusoidal clock input a generate clean square waves with fast transitions at all but the highest frequencies. The outputs of the three buffers are dotted together to eliminate any clock skew that may be introduced between the three, however due to their small

size and careful floorplanning such effects should be minimal. This floorplaning can be seen through the 2 to 1 MUX layout in Figure 8.2.

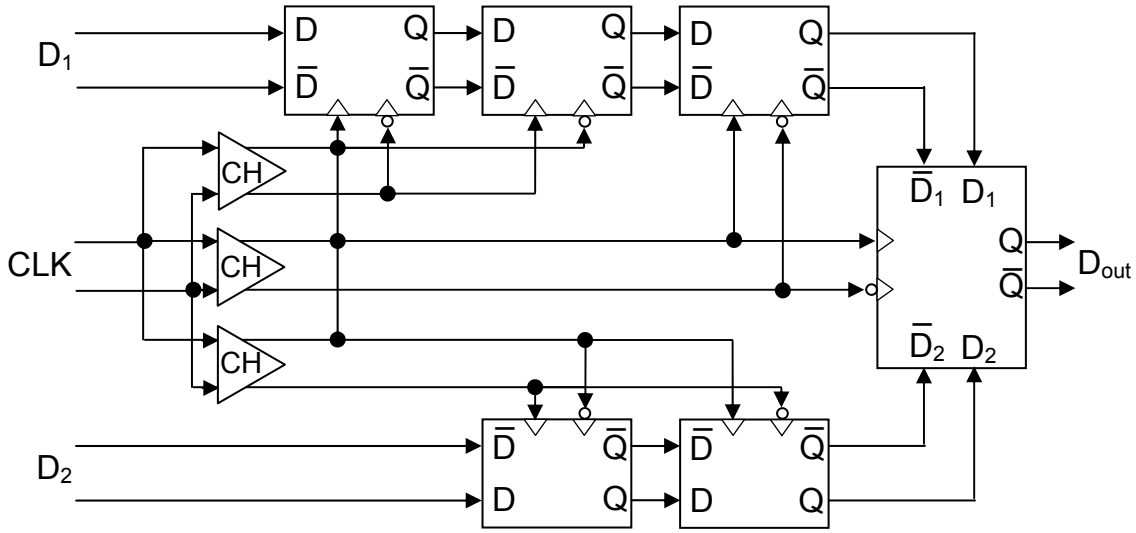



Figure 8.1: 100 GB/s 2 to 1 MUX Schematic

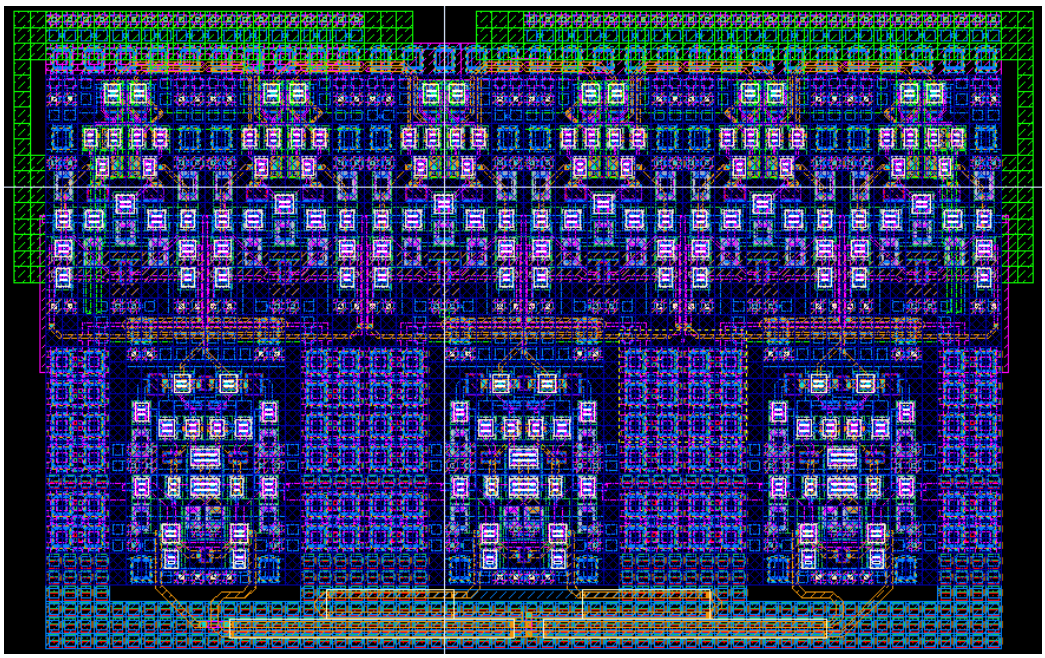
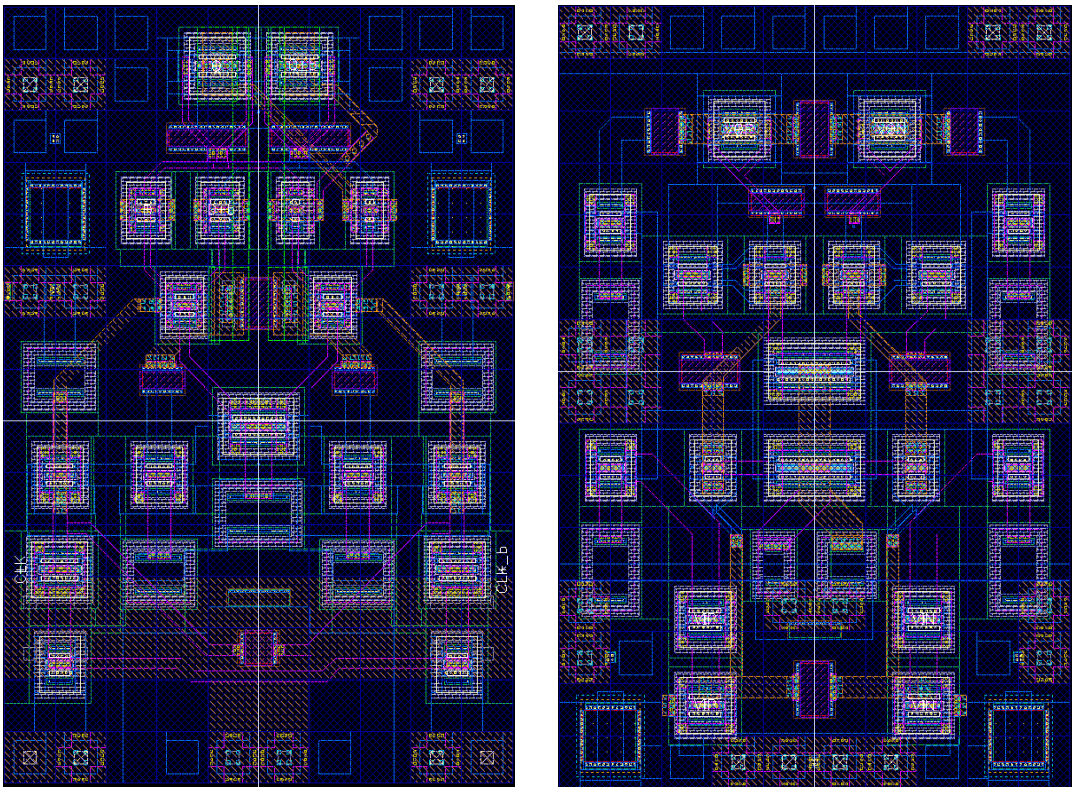


Figure 8.2: 100 GB/s 2 to 1 MUX Layout

In Figure 8.2 the three parallel clock buffers can be seen in the bottom half of the circuit, with the latches and selector on the top. To properly drive the inputs of the three buffers and the latches (selector) all the wiring must be electrically matched, hence the use of the bent transmission lines throughout the clock structure. The subcircuits employed were laid out to minimize the amount of wiring needed, both internal to their structure and to wire between the different components. Close-ups of the Latch and Cherry Hooper Buffer can be seen in Figure 8.3 (the selector is omitted as it has a very similar layout to the latch).




(a) (b)

Figure 8.3: (a) mmWave Latch and (b) Cherry Hooper Buffer Layouts

All of the components within the MUX are designed to occupy a space of exactly 75 μm and 50 μm, minimizing interstage wiring and adding flexibility to the design process. In Figure 8.3 (a) the input and output (D and Q) of the latch are both at the top center of the cell, which eliminates the need to wire across all the bias and clock circuitry when connecting multiple latches together. Due to the compact nature of these cells the entire MUX can be realized in an area of 300 μm by 190 μm, with unused space occupied by decoupling and power distribution.

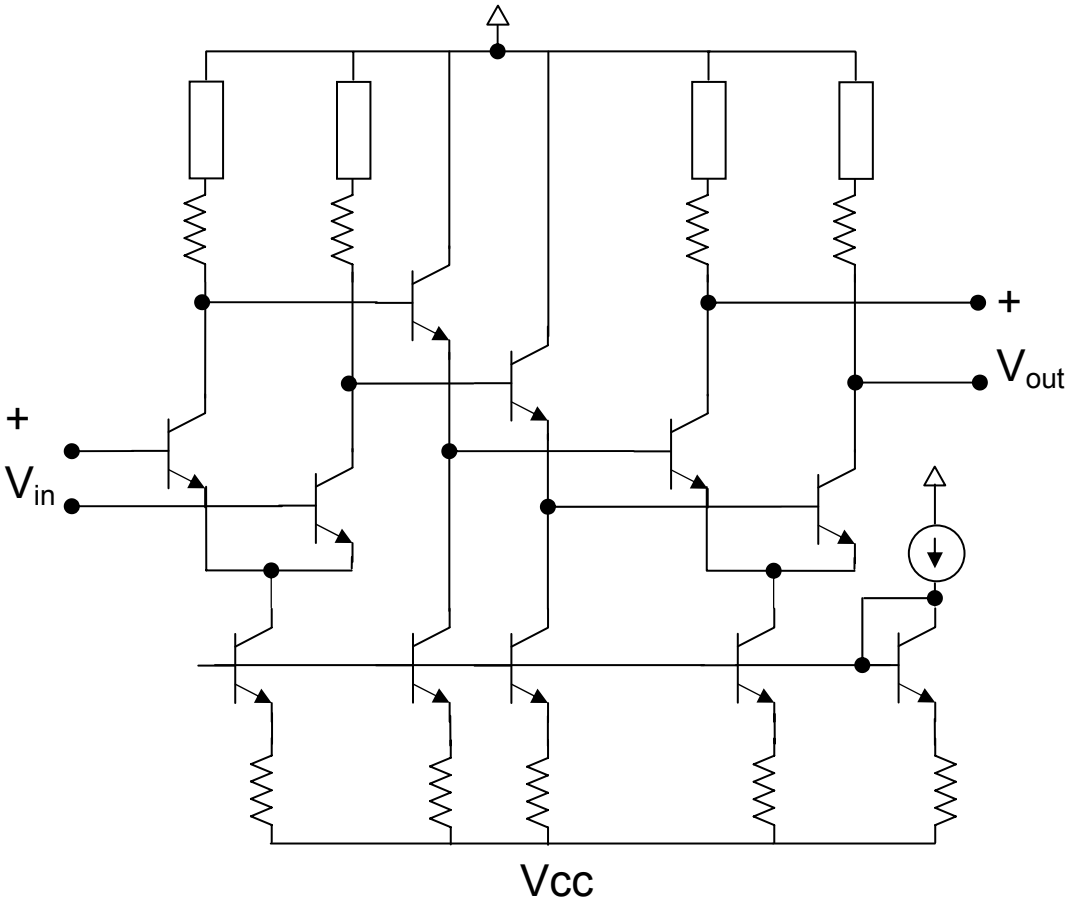



Figure 8.4: Full Rate MUX Output Buffer Schematic

As was mentioned previously the 4 to 1 MUX was constructed using three 2 to 1 MUXs, two of them operating from a quarter rate clock and one from a half rate clock. Additional circuitry was added to create the 4 to 1 MUX includes additional buffers for the signal and clock inputs and distribution, and a high power output buffer to operate at full rate (the only subcircuit required to do so). For both the signal and clock inputs the pads were wired directly into emitter followers to enable high frequency operation and 50 Ω matching, with an intermediate emitter-coupled pair at the signal inputs to increase the operating range down to lower input power levels. The output buffer used two stages of peaked emitter-coupled pairs connected with emitter followers (for level shifting), for the topology shown in Figure 8.4. The layout of the full-rate output buffer can be seen in Figure 8.5.

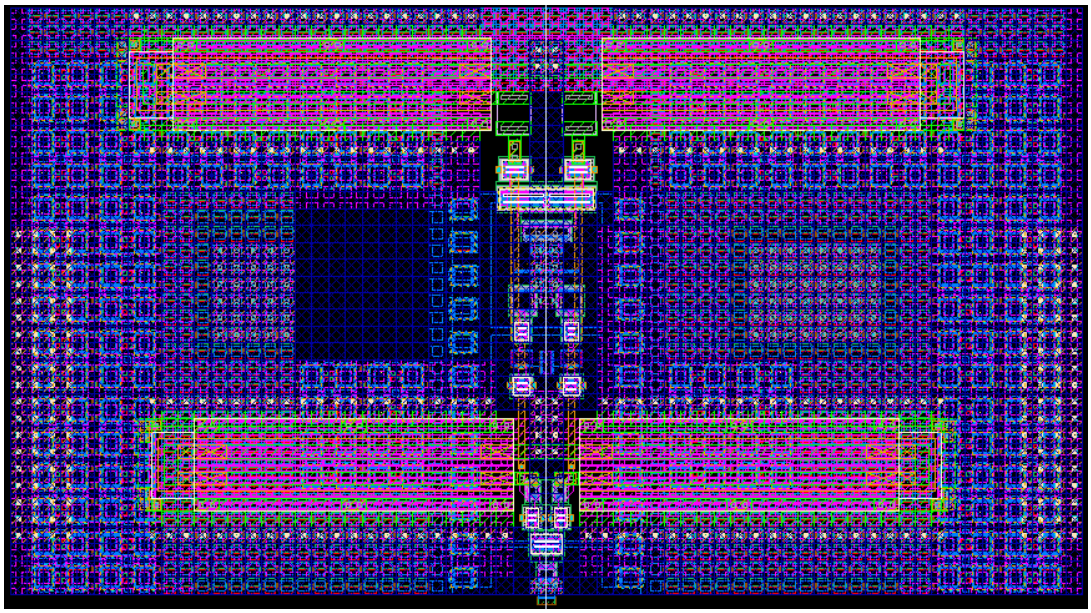


Figure 8.5: Full Rate MUX Output Buffer Layout

In Figure 8.5 the signal flows from the inputs to outputs from the bottom of the layout to the top. Here it can be seen that the transmission lines employed for peaking applications are folded back to meet along the buffers access of symmetry, which generates an accurate common mode node eliminating resonances due to un-modeled return paths.

Assembling these components, and adding a mmWave power structure as described in previous designs, the 4 to 1 MUX is assembled as seen in Figure 8.6.

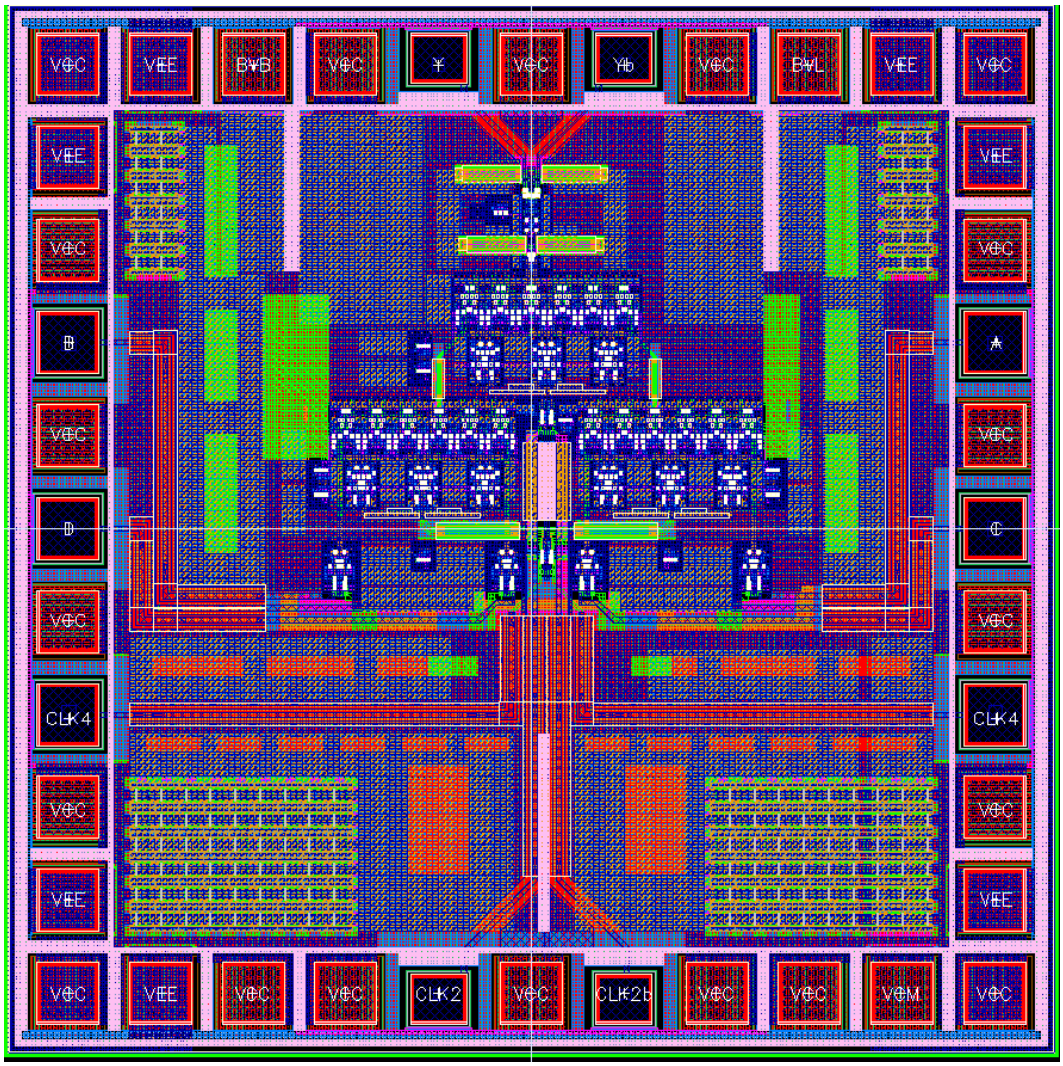



Figure 8.6: 100 GB/s 4 to 1 MUX Layout

In the MUX of Figure 8.6 it can bee seen that substantial area is occupied by only decoupling and transmission lines, to fill a geometry who's size is mandated by the number of pads required. In the circuit it can bee seen that the half rate clock is delivered from the bottom of the chip, the quarter rate clock and signal inputs from the sides, and the full rate output at the top. This is done to put the high speed pads (for clock and output) opposite each other on the chip, easing test and packaging of the finished die. Also, in so doing the additional lengths of wire needed to connect the highest speed pads are minimized, reducing parasitics on the most sensitive nodes. It is for this reason that the MUX is located at the top of the die, so that the length of wire on the full rate signal output is at an absolute minimum.

### 8.1.2 Experimental Results

While test results for the wireline samples are not available (as they are still being fabricated), thorough simulation results can demonstrate the high data rates possible by employing mmWave techniques to conventional architectures. Simulation results of the 4 to 1 MUX, with input data rates from 5 GB/s to 25 GB/s (output rates from 20 GB/s to 100 GB/s) are shown in Figure 8.7. The MUX consumes 590 mA from a 3.3V supply, but can operate as low as 3 V (up to 60 GB/s). At maximum rate the MUX experiences less than 1.5 ps of jitter with less than 5 % eye closing due to ISI. The overshoot experienced at the lower data rates is a result of the inductive peaking employed in the output buffer, and minimizing that overshoot by reducing the peaking is the primary factor limiting the maximum data rate.

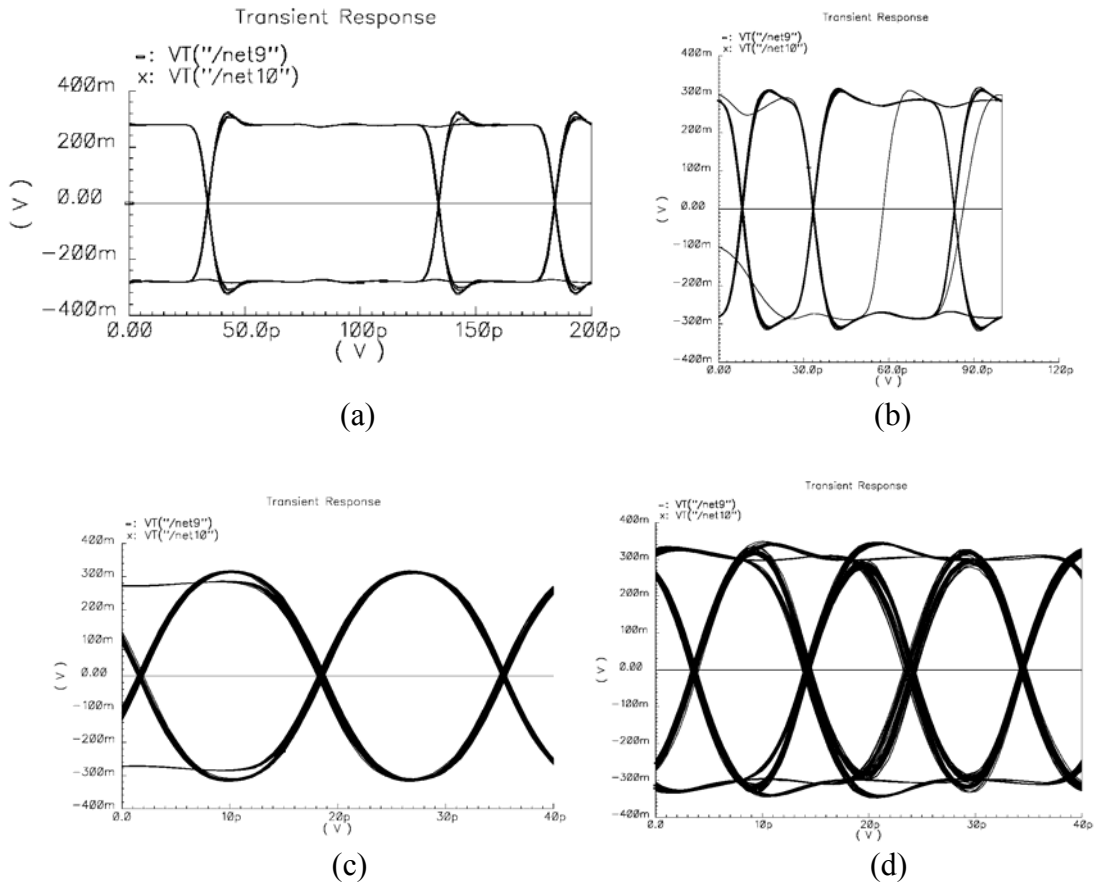



Figure 8.7: 4 to 1 Mux output eye diagrams at (a) 20 GB/s output rates, (b) 40 GB/s output rates, (c) 60 GB/s output rates, and (d) 100 GB/s output rates

## *8.2 1 to 4 DeMUX*

### 8.2.1 Design and Layout Considerations

Similar to the 4 to 1 MUX, the 1 to 4 DeMUX uses three 1 to 2 DeMUXs cascaded together, with separate clocks provided at half-rate and quarter-rate, with no full rate clock. A schematic of the 1 to 4 DeMUX can be seen in Figure 8.8 [54,55].

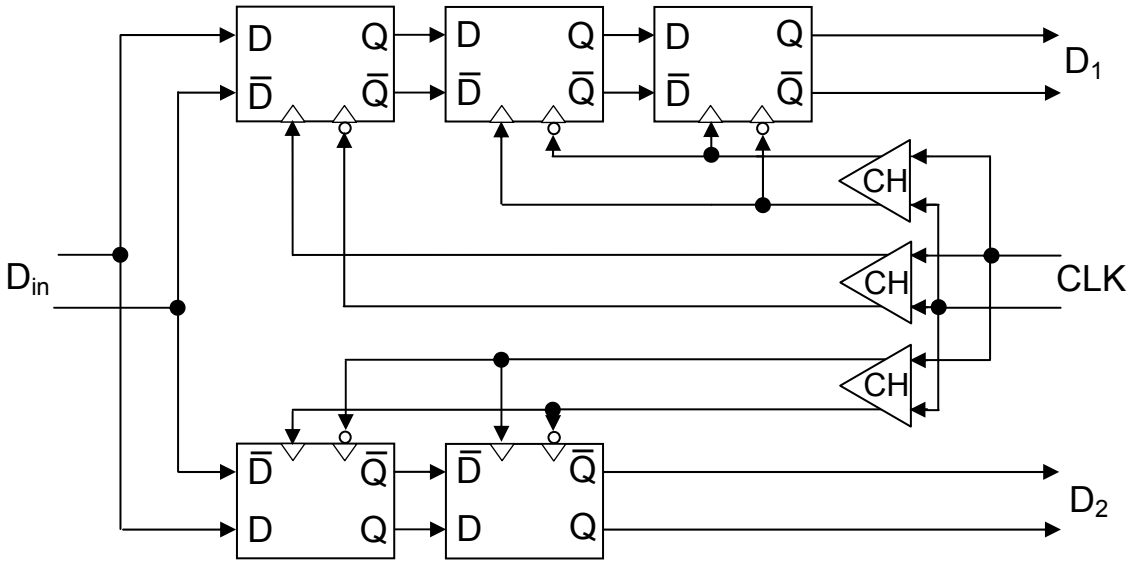



Figure 8.8: 100 GB/s 1 to 2 DeMUX Schematic

Similar to the MUX in the components used (Cherry-Hooper buffers and asymmetric latches), the DeMUX differs due to the different architecture. Since no selector is employed, there are an odd number of ECL gates, meaning that if three buffers are employed they will not have equivalent fanout. This can be seen for the input latch of the $D_1$ path, where the latch has its own clock buffer. This can introduce some asymmetry to the circuit as the Cherry-Hopper buffer may experience a different clock delay when driving a different load (less capacitive to drive a single gate than to

drive two), and the latches may respond differently under a larger clock swing (since the clock power isn't divided between two latches). Another difficulty of the DeMUX is inherent in the floorplan possible of the 2 to 1 MUX. Due to spacing between like outputs of the clocking network, dotting together the clock signals between the Cherry-Hooper buffers isn't possible without introducing a significant amount of wire (which would defeat the purpose of doing so), making this circuit more susceptible to clock skew. The layout of the 1 to 2 DeMUX can be seen in Figure 8.9.

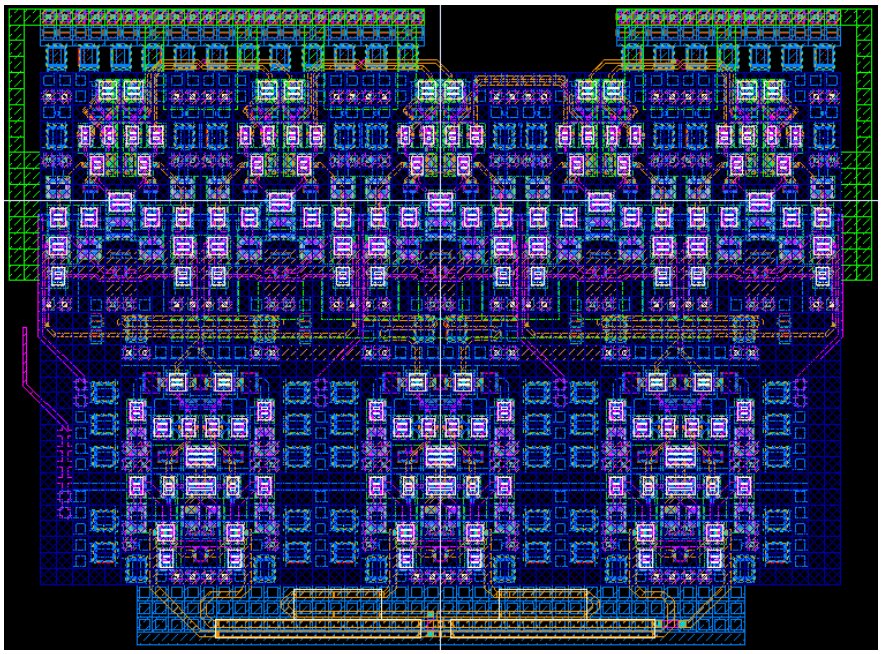


Figure 8.9: 100 GB/s 1 to 2 DeMUX Layout

In Figure 8.10 the DeMUX uses a floorplan very similar to that of the MUX, with the clock buffers arrayed across the bottom of the cell and the latches placed linearly across the top to minimize wiring. Again phase matched wiring is required for every interconnect to ensure symmetrical operation, and excess space is used for decoupling and power distribution.

Unlike in the 4 to 1 MUX the full rate connection for the 1 to 4 DeMUX is the input, requiring a different buffer than that used in the MUX. To ensure sensitivity to low input power levels while matching to 50 Ω across the entire bandwidth two stages of Cherry-Hooper buffers were used, slightly detuned from those used in the clock network (larger feedback resistances) to increase stability. The layout of the 1 to 4 DeMUX can be seen in Figure 8.10, where the floorplan is identical to that of the 4 to 1 MUX, only with the inputs and outputs reversed.

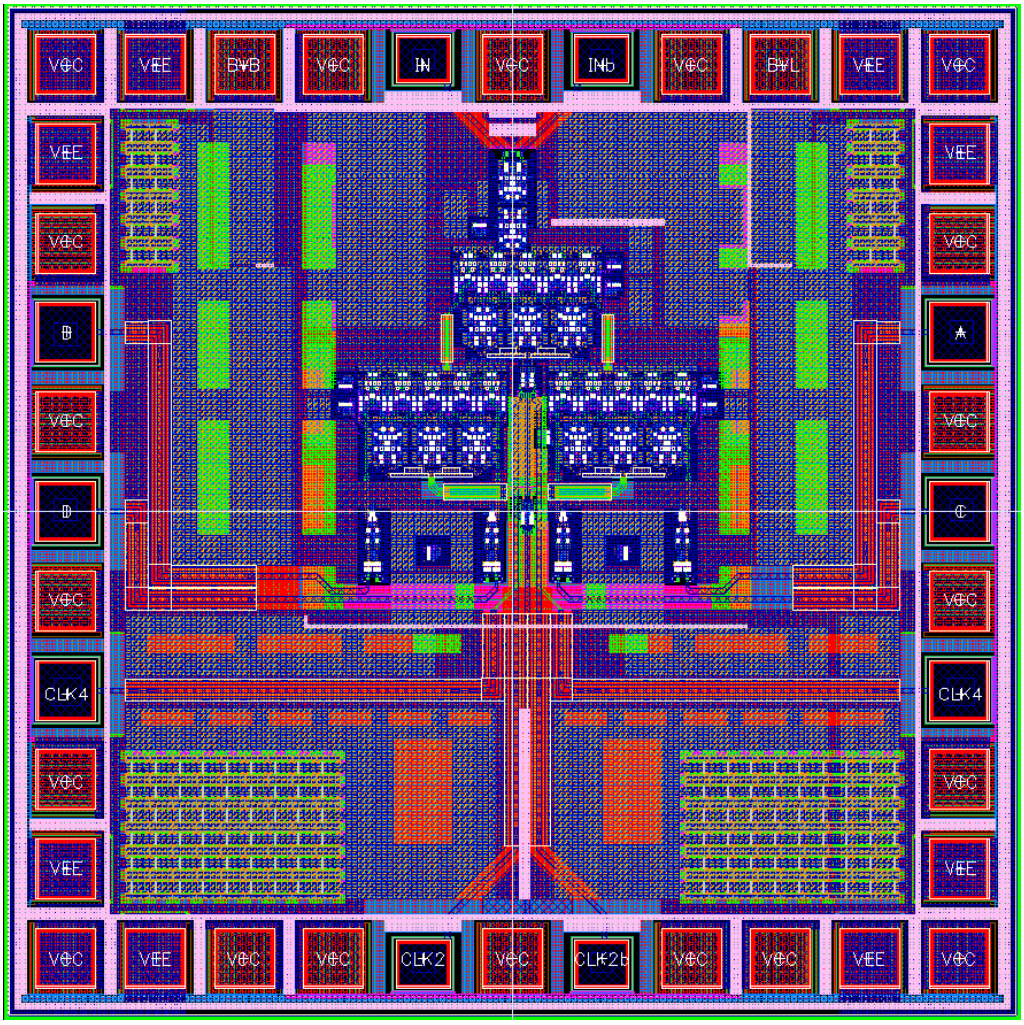



Figure 8.10: 100 GB/s 1 to 4 DeMUX Layout

Here again a significant amount of the chips area contains only decoupling, used to consume the extra space needed to accommodate the necessary number of pads. In both cases many of the pads required are for DC controls and supplies, especially as in the case of the later redundant contacts are needed to accommodate the large current consumption of the chip. That considered, the determining factor for the size of the padframe in both of these chips is the package technology used, ribbon bonded ceramic packages, as different package technologies (flip-chip on glass) would allow for smaller pads, dramatically decreasing the size of the chip and potentially increasing the bandwidth of the output buffers.

### 8.2.2 Experimental Results

Simulation results of the 1 to 4 DeMux, with input data rates from 20 GB/s to 100 GB/s (output rates from 5 GB/s to 25 GB/s) are shown in Figure 8.11. The DeMux consumes 460 mA from a 3.3V supply, but can operate as low as 3 V (up to 60 GB/s).

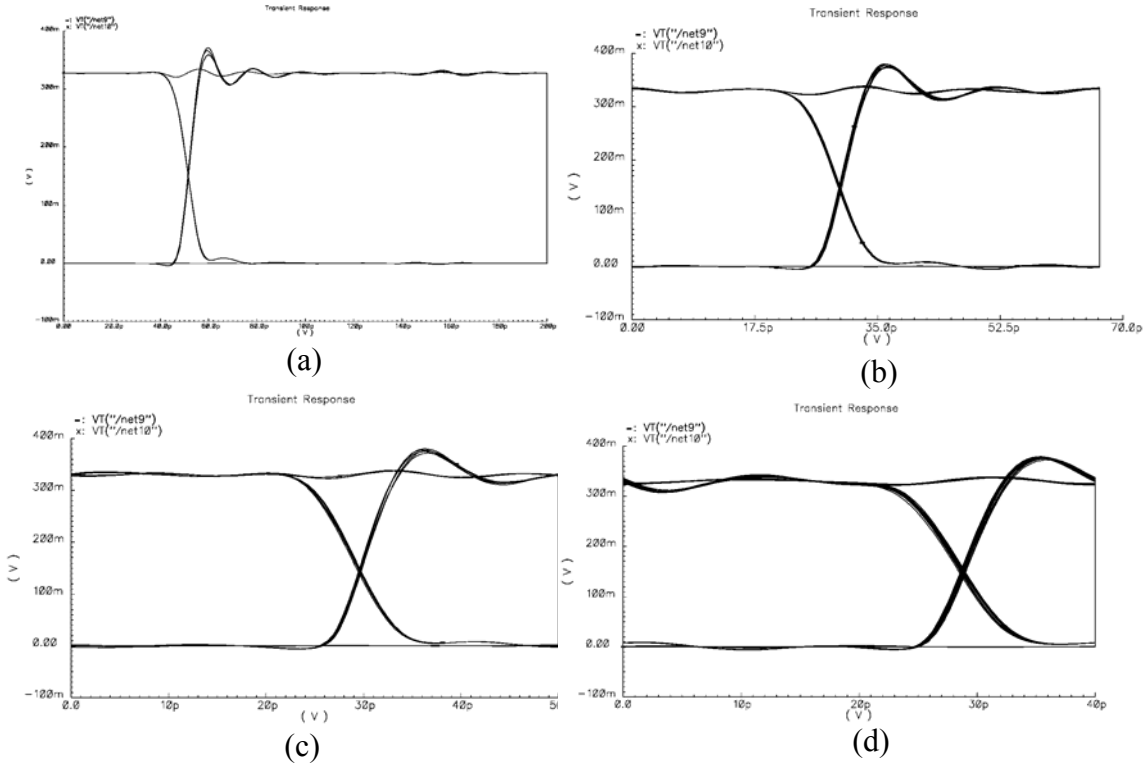



Figure 8.11: 1 to 4 DeMux output eye diagrams at (a) 20 GB/s input rates, (b) 60 GB/s input rates, (c) 80 GB/s input rates, and (d) 100 GB/s input rates

## *8.3 Static Divider and DFF Design*

### 8.3.1 Design and Layout Considerations

Similar to the design topologies discussed in Chapter 6, a static divider and DFF (D Flip Flop) were designed for operations peripheral to the MUX and DEMUX (package level system design) and for verification of the bandwidth of the employed components (the static divider is a useful circuit for verifying the operation of the latches). The components were kept separate from the MUX and DEMUX to give greater flexibility (as per the design requirements) and hopefully allow for a broader

MUX/DeMUX response (as the divider is typically the limiting factor in the operation of these systems). Schematics of the two circuits can be seen in Figures 8.12 and 8.13.

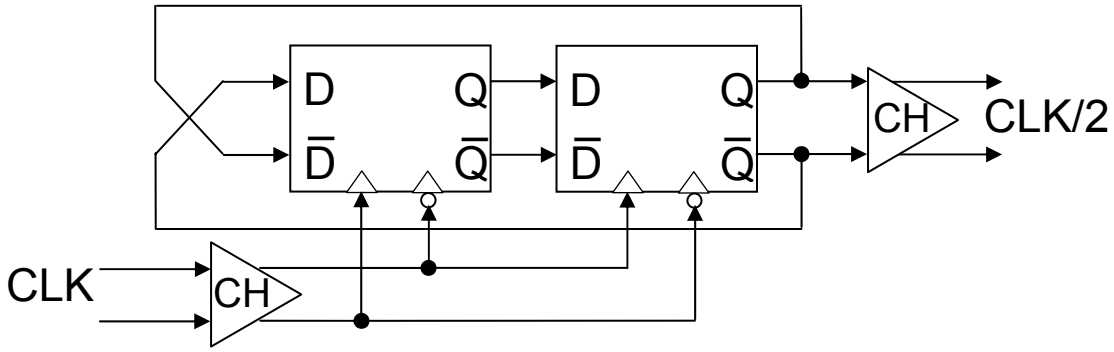



Figure 8.12: 60 GHz Static Divider Schematic

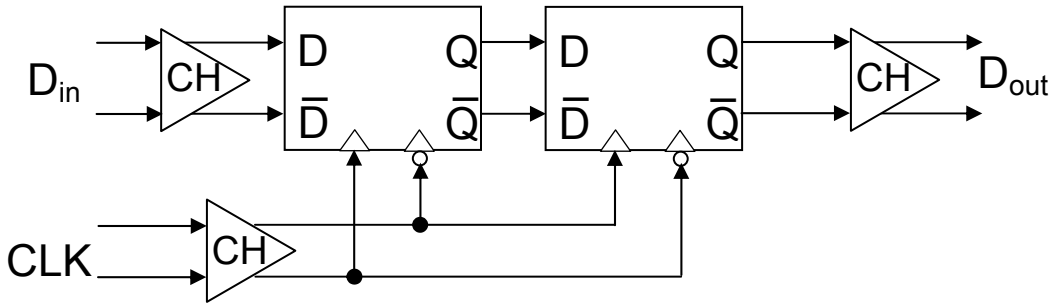



Figure 8.13: 60 GHz DFF Schematic

Because these two circuits use the same footprint as employed in the MUX and DEMUX, much of the area of the die is consumed only by power distribution and decoupling. This is more of a limiting factor in these elements than the MUX and DEMUX because their small size dictates much longer interconnects to reach the pads, and their I/O's are at a higher frequency (especially the DFF, with two full rate signal lines). Layouts of the two circuits can be seen in Figures 8.12 and 8.13.

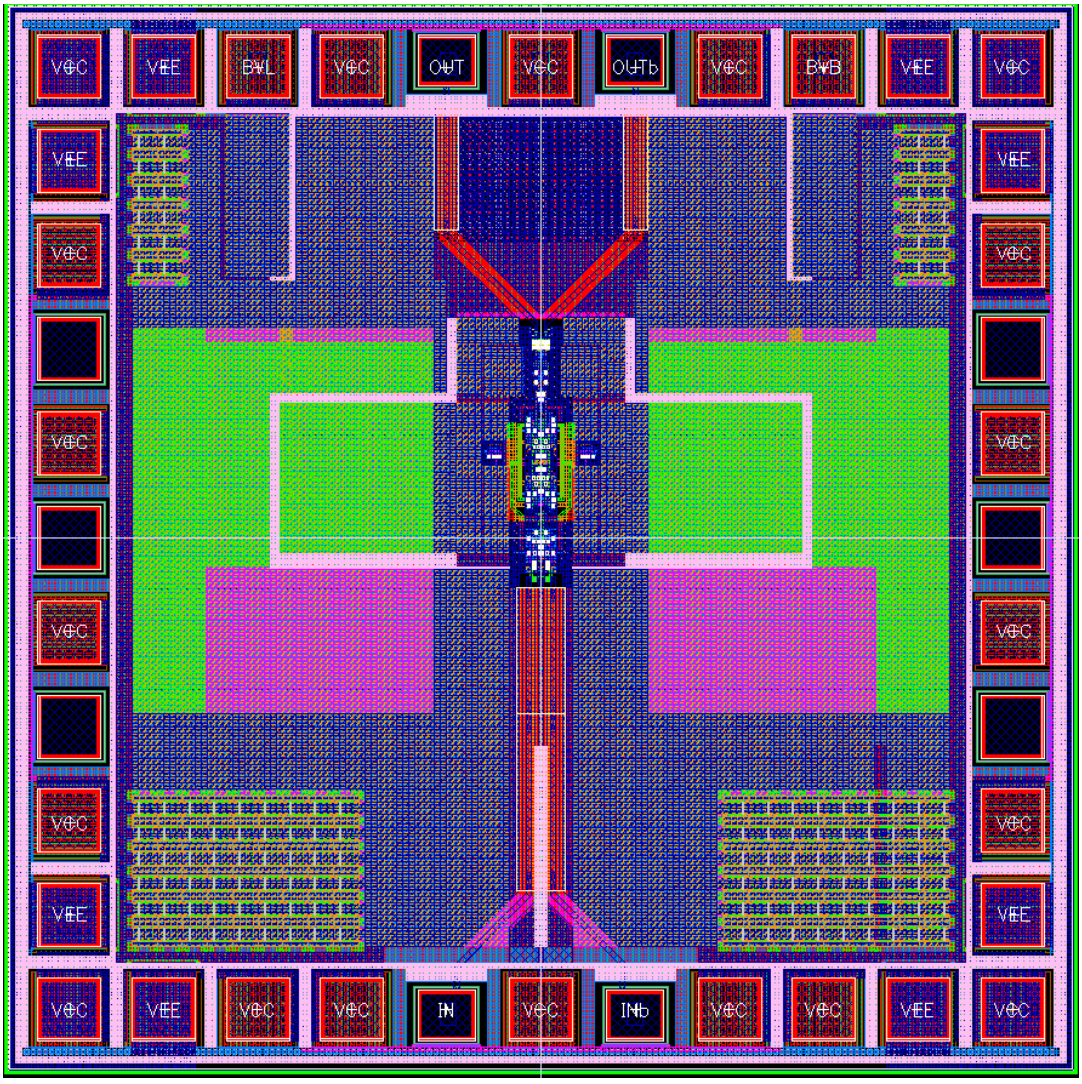



Figure 8.14: 60 GHz Static Divider Layout

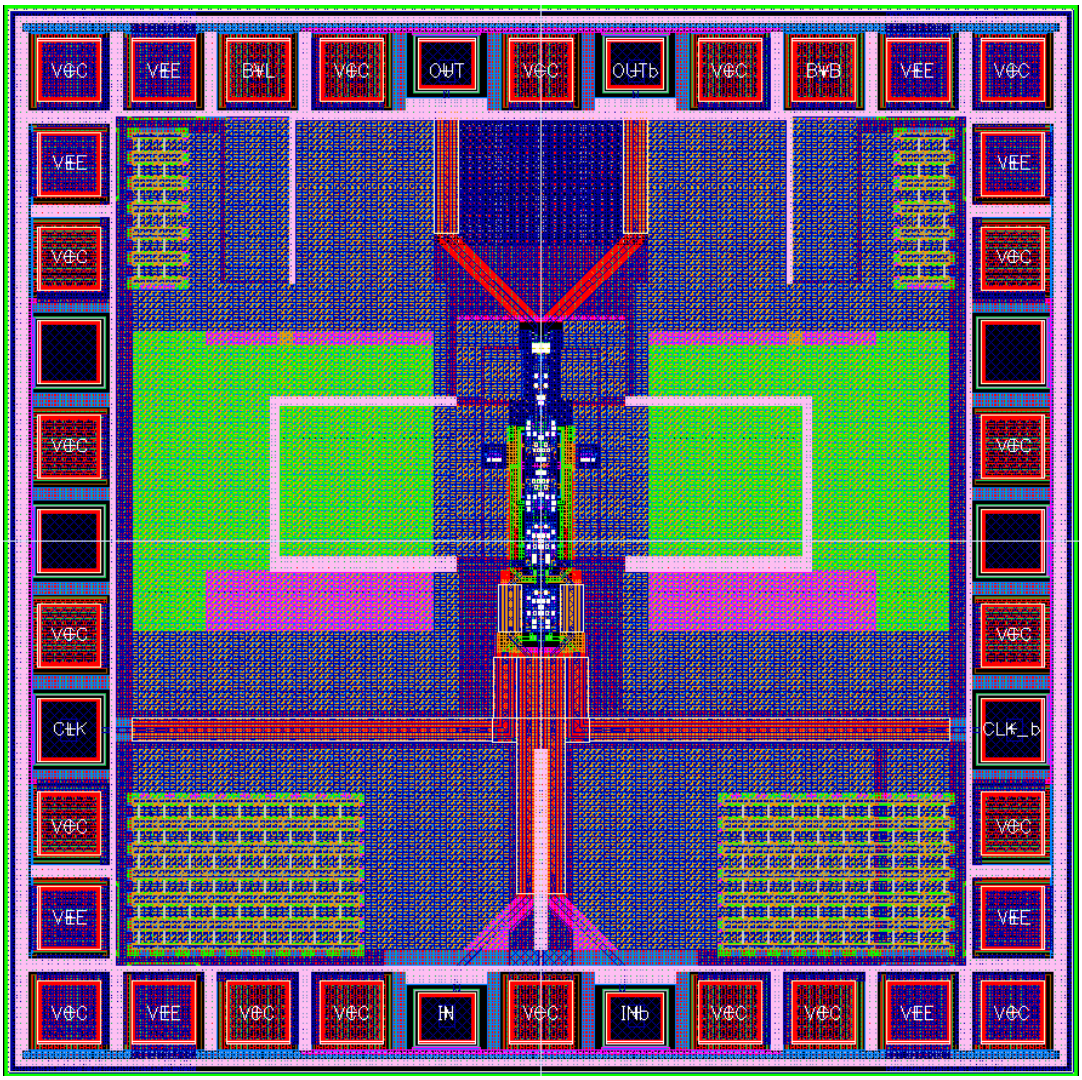



Figure 8.15: 60 GHz DFF Layout

### 8.3.2 Experimental Results

Simulation results of the static divider and DFF can be seen in Figures 8.16 and 8.17. Here the divider is shown to operate (dividing by two) up to 60 GHz while consuming 80 mA of current from a 3.3V supply. The DFF operates up to 60 GB/s (although significant ISI and Jitter is present at higher data rates) while consuming 250 mA of current from a 3.3 V Supply.

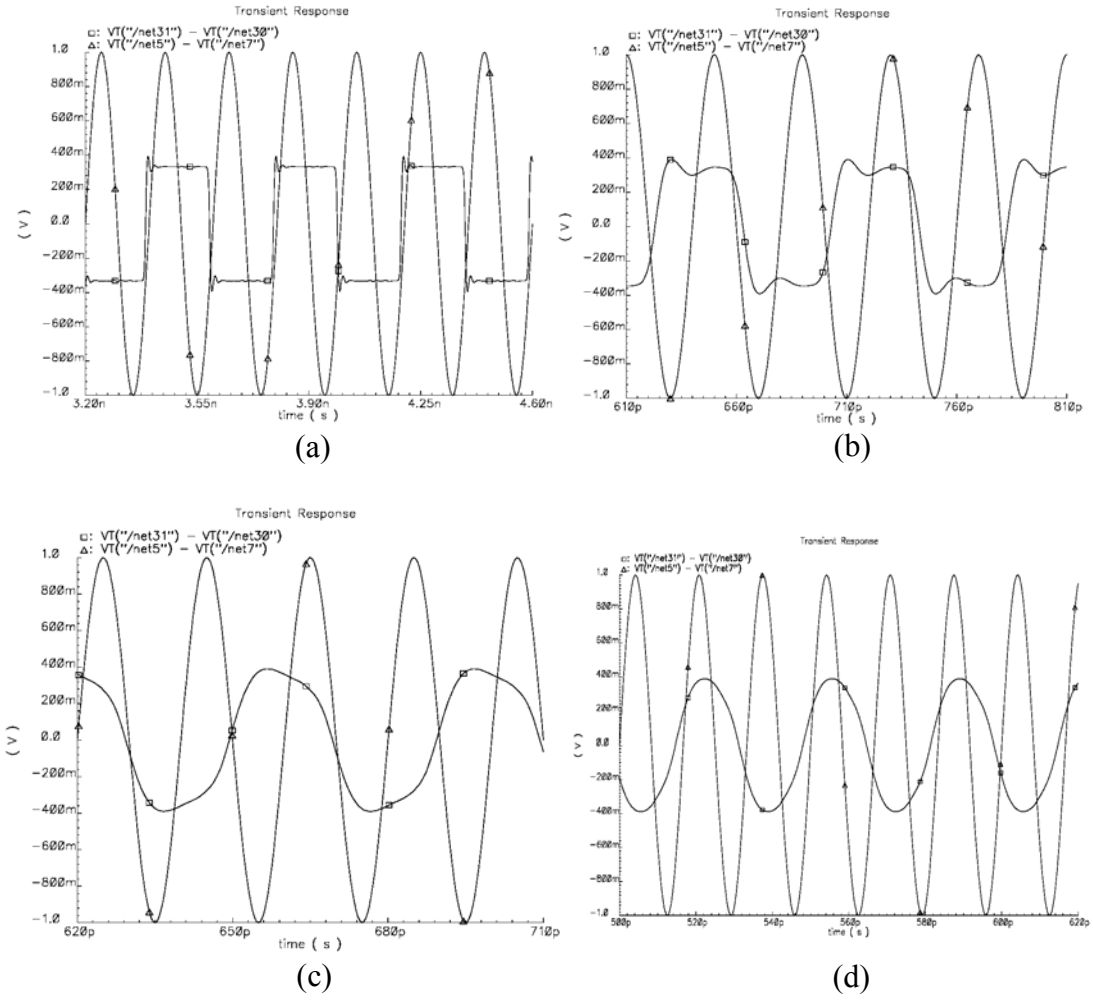
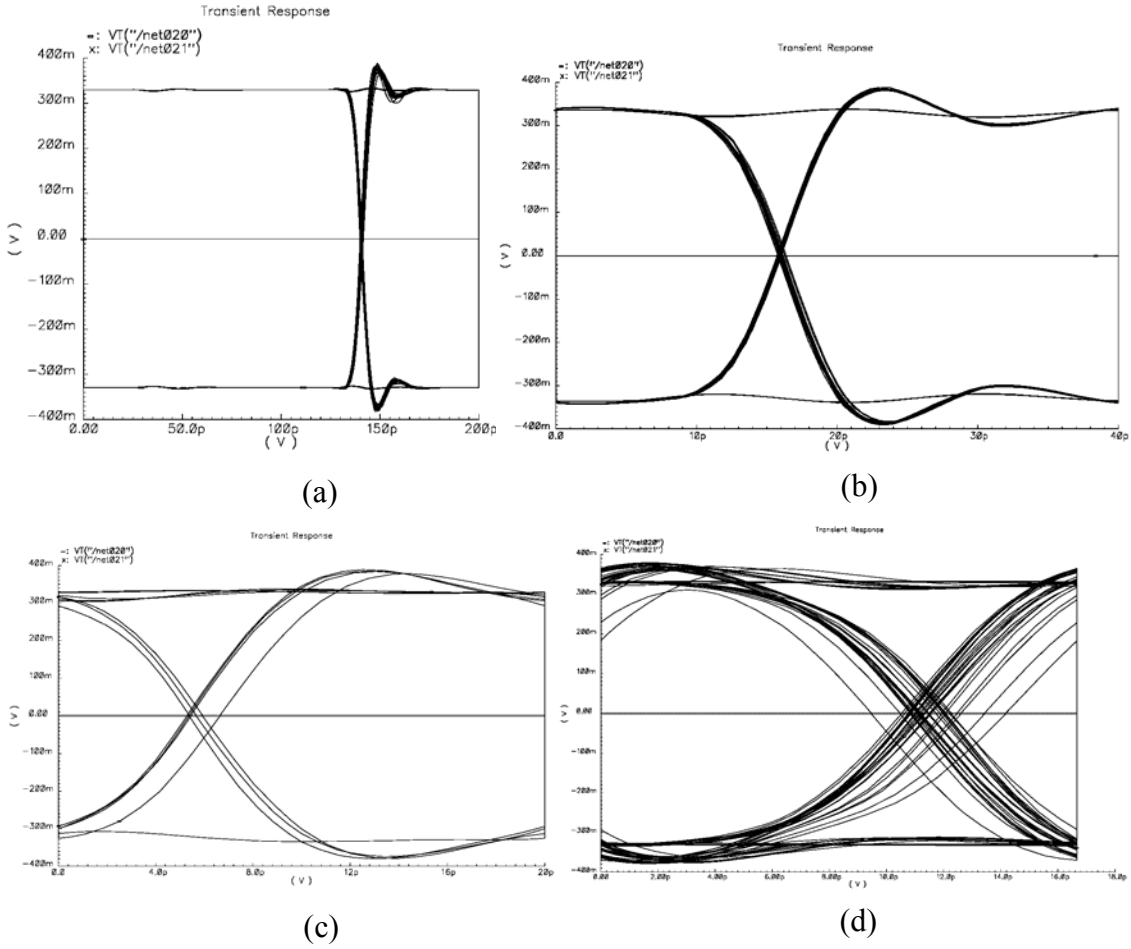



Figure 8.16: Static Divide by two with (a) 5 GHz input rate, (b) 25 GHz input rate, (c) 50 GHz input rate, and (d) 60 GHz input rate (input signal shown with Δ, output signal with □)




(a) (b)

(c) (d)

Figure 8.17: DFF at (a) 5 GB/s, (b) 25 GB/s, (c) 50 GB/s, and (d) 60 GB/s

## 8.4 Conclusions

A family of circuits was built for mmWave wireline communication applications up to 100 GB/s. Here a 4 to 1 MUX and it's companion 1 to 4 DeMUX were demonstrated to operate across a very broad range of data rates (from inputs of a few GB/s to outputs of 100 GB/s) under reasonable power consumptions, consuming less than 20 mW per GB/s. Complimentary to these circuits were a static divider and

DFF both capable of operation up to 60 GHz (60 GB/s for the DFF), enabling package level construction of more novel wireline systems. Together these circuits represent the fastest family of silicon wireline communication circuits yet developed, and approach those data rates presently capable only through more exotic substrates (GaAs, InP) [54,55,56,57].

# Chapter 9 Conclusions

## *9.1 Summary of this Work*

In this work the methods necessary for mmWave design in Silicon technologies are explored, with distinctions drawn between them and conventional high speed design practices. These methods, which derive from the increased susceptibility of components to variation at high frequency, are distinct in that they identify and resolve the shortcomings of a technology beyond limitations of the speed of a device. The ultimate result is the identification of these risks inherent in electrically complex designs, and a proposal for new techniques to counter the compromises to the electrical circuit through creative use of passive elements and intelligent floorplanning.

While separate techniques are developed for the different circuits described herin, the fundamental tenant underlying the advancement of these circuits and systems is the reduction in size of the active areas of the designs. This effort works to combat the effects of unwanted and unknown parasitics, reducing design variability and excessive bandwidth restrictions. Also common to these designs is the aggressive scaling of device sizes to mitigate the effects of device capacitances, which have been shown not to scale with the maximum transit frequency of a transistor and hence lead to bandwidth restrictions and corruption of the validity of small signal models.

One example of a conventional technique used at high frequencies (especially in SiGe technologies) that is a limitation at mmWave is the use of AC coupling in the feedback of a VCO. By enabling level shifting this technique allows a circuit to be biased to inhibit saturation, however at high enough frequencies parasitics exhibited by the capacitors necessary to implement this unnecessarily slow the circuit. This behavior is a direct extension of the previously mentioned benefits of the reduction of

the active area of a circuit, and even this concept of AC vs. DC coupling can be extended beyond the VCO to realize bandwidth improvements in other circuits. Common to all designs described within this work is the employment of the most electrically simple circuit that would perform the given task, to eliminate the excess wiring necessary to accommodate large numbers of active devices and therefore reduce the risk of performance deviations due to extraction inaccuracies.

While certain limitations are placed on monolithic mmWave circuit and systems design due to the quality of the back end, these limitations are offset and in many cases overcome due to the difficulty inherent in transitioning between substrates at these frequencies. It is for that reason that while any one passive element could be implemented off chip to achieve a higher quality, that improvement would vanish when the effects of the interconnect (pad, C4, wirebond, etc.) are considered. This reveals one of the greatest benefits of mmWave silicon design, in that the ability to integrate an entire system onto a single chip removes the limitations of communicating between substrates inherent in other platforms (GaAs, InP, etc.).

Using these understandings circuits were demonstrated to show the viability of mmWave design (in Silicon) in both wireless and wireline systems. VCOs were developed into the 60 GHz ISM band with exceptional abilities regarding both power and noise, and LNAs surpassed their frequency with performance up to (and beyond) 94 GHz. Wireline development saw the first silicon MUX/DeMUX family developed for operation above 100 GB/s, with a complimentary divider and DFF for more advanced system design.

## *9.2 Technology Hurdles*

While the work presented here demonstrates ways to cope with the limitations of silicon technologies, especially those peripheral to the performance of the

transistors, these techniques are merely a stopgap in the move towards more advanced technologies. While substantial effort has been exerted into the improved speed of the transistors, the technologies have lagged in many other regards. Foremost, limitations in the back end, which encompasses all of the wiring and dielectric used to generate capacitors and transmission lines, seriously inhibit the ability to have high quality tanks or low loss signal distribution. With these improvements to silicon technologies the need to take efforts to avoid the use of complicated electrical circuits, the so called conventional high speed technique, would be mitigated and more options would be made available to the designer. That considered, these same techniques could also be employed within an improved technology to create even faster components, potentially allowing the technologies to finally unleash the true potential of their devices.

## 9.3 Future Work

While it is possible to envision applications of this work into many areas of analog and digital design, the near future of this work resides mainly in advanced communication technologies. By developing mmWave silicon transceivers to provide wireless data rates up to (and beyond) 20 GB/s a low cost solution would be available for any high density networking applications, or low infrastructure datacom solutions. While this work is a first step, it demonstrates the techniques necessary to achieve these systems, and with their deployment there are few hurdles to a single chip silicon solution for all realistic wireless communication needs.

The wireline work is indicative of a resurgence in the need for faster wired communication links, and is portable between wired or optical solutions. Its largest potential application, beyond its myriad of uses as a test element for other circuits, is in handling the increasing need for communication between systems in massively

parallel computers. By increasing the data rates tenfold beyond those conventionally employed today the limitation placed on these systems by their inability to accommodate the necessary transfer rates would be diminished, and by removing so much necessary infrastructure from the system costs would be driven lower.

Beyond these obvious uses mmWave silicon has near unlimited potential, be it in the form of automotive radar systems for adaptive cruise control, military and medical imaging, or potentially even noninvasive medical therapeutics. While these uses may only be realized far off into the future, it is this author's opinion that growing interests in these fields will help spur new competition and subsequent rewards in markets not typically associated with silicon advancement.

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